SSD1355

Advance Information

128 RGB x 160 Dot Matrix
OLED/PLED Segment/Common Driver with Controller

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1 GENERAL DESCRIPTION

The SSD1355 is a CMOS OLED/PLED driver with 384 segments and 160 commons output, supporting up to 128RGB x 160 dot matrix display. This chip is designed for Common Cathode type OLED/PLED panel.

The SSD1355 had embedded Graphic Display Data RAM (GDDRAM). It supports with 8, 16, 18 bits 8080 / 6800 parallel interface, Serial Peripheral Interface. It has 256-step contrast and 262K color control, giving vivid color display on OLED panels. This driver IC can be used in many different applications such as MP3, PDA, PMP, mobile phone and Digital Camera.

2 FEATURES

- Resolution: 128 RGB x 160 dot matrix panel
- 262k color depth supported by embedded 128x160x18 bit SRAM display buffer
- Power supply
  - V_{DD} = 2.4V – 2.6V (Core V_{DD} power supply, can be regulated from V_{CI})
  - V_{DDIO} = 1.6V – V_{CI} (MCU interface logic level)
  - V_{CI} = 2.4V - 3.5V (Low voltage power supply)
  - V_{CC} = 10.0V – 21.0V (Panel driving power supply)
  - When V_{CI} is lower than 2.6V, V_{DD} should be supplied by external power source
- Segment maximum source current: 200uA
- Common maximum sink current: 80mA
- 256 step brightness current control for the each color component plus 16 step master current control
- Pin selectable MCU Interfaces:
  - 8/16/18 bits 6800-series parallel interface
  - 8/16/18 bits 8080-series parallel interface
  - 3 –wire and 4-wire Serial Peripheral Interface
- Support various color depths
  - 262k color (6:6:6)
  - 65k color (5:6:5)
- OLED Driving Scheme: PAM + PWM
- Three programmable Gamma Look Up Tables (GLUT) for red, green and blue. Each GLUT entry size is 7-bit.
- RAM write synchronization signal to avoid flickering when updating new image
- Sleep mode current <10uA with ram data kept
- Non-volatile memory (OTP) for panel calibration
- Row re-mapping and Column re-mapping
- Horizontal and Vertical scrolling
- Programmable Frame Rate and Multiplexing Ratio
- On-Chip Oscillator
- High Power Protection
- Color Swapping Function (RGB – BGR), arranged in RGB sequence when reset
- Slim chip layout for COF
- Operating temperature range -40°C to 85°C.

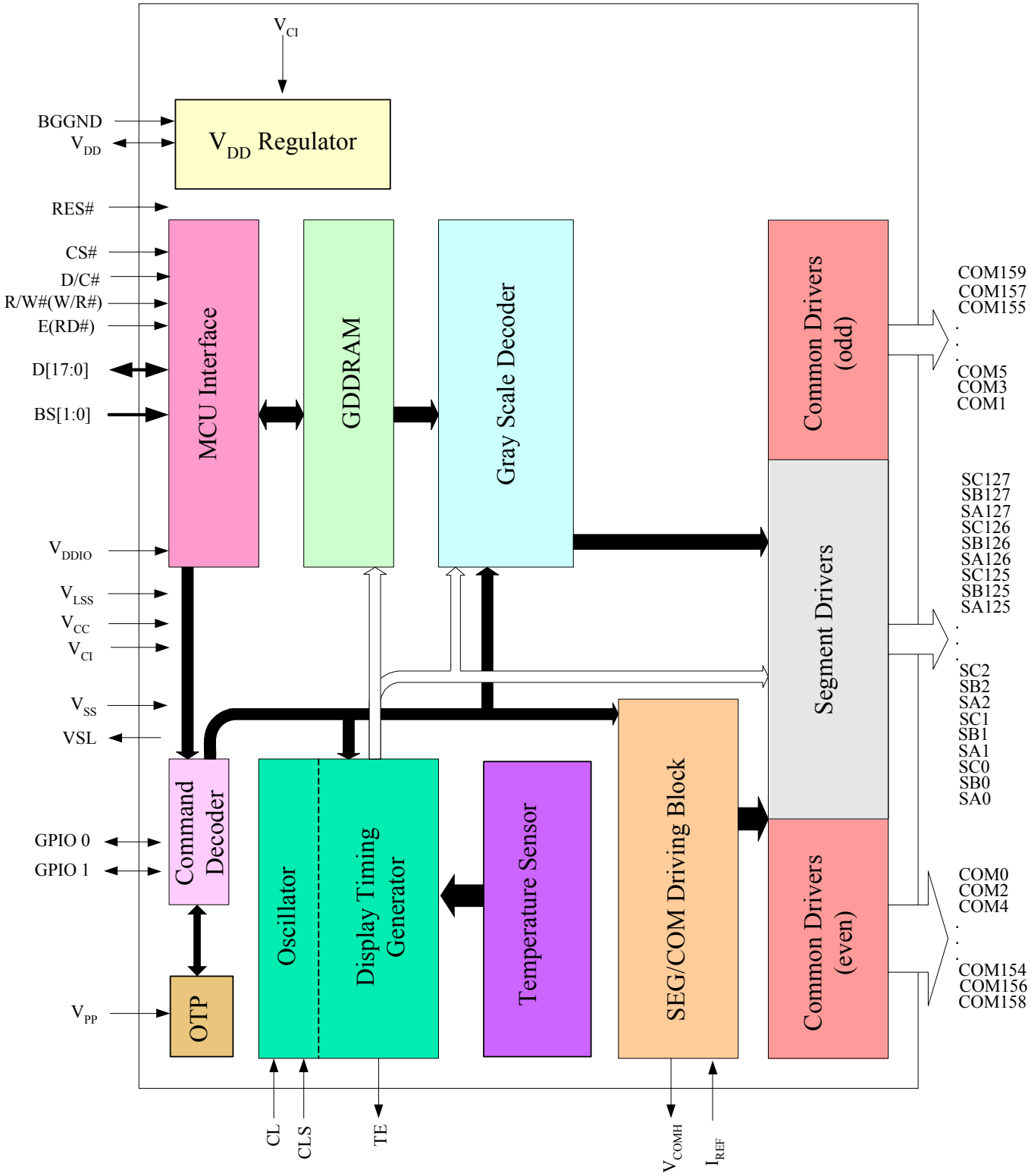
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

Ordering Part Number	SEG	COM	Package Form	Reference	Remark
SSD1355Z	128RGB	160	Gold Bump Die	Page 9	• Min SEG pad pitch : 27um • Min COM pad pitch : 35um
SSD1355U2R1	128RGB	128	COF	Page 12, 105	• 35mm film, 4 sprocket hole • Hot bar type COF • 16/8-bit 80/68/SPI interface • SEG lead pitch 0.051mm x 0.999 = 0.050949mm • COM lead pitch 0.051mm x 0.999 = 0.050949mm
SSD1355U3R1	128RGB	96	COF	Page 15, 107	• 35mm film, 4 sprocket hole • Hot bar type COF • 8-bit 8080/6800 interface • SEG lead pitch 0.053mm x 0.999 = 0.052947mm • COM lead pitch 0.053mm x 0.999 = 0.052947mm
SSD1355U6R1	128RGB	160	COF	Page 18, 109	• 48mm film, 4 sprocket hole • Hot bar type COF • 16/8-bit 80/68/SPI interface • SEG lead pitch 0.059mm x 0.999 = 0.058941mm • COM lead pitch 0.059mm x 0.999 = 0.058941mm

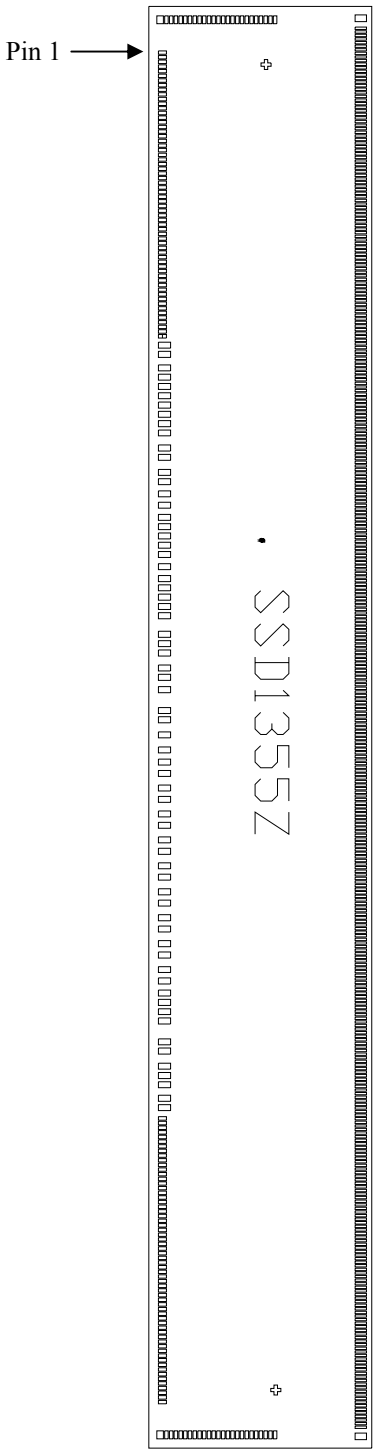
4 BLOCK DIAGRAM

Figure 4-1 Block Diagram



5 DIE FLOOR PLAN

Figure 5-1 : SSD1355Z Die drawing



Alignment marks

	Position	Size
+ shape	(-4988.93 , 42.65)	75um x 75um
+ shape	(4988.93 , 14.46)	75um x 75um

Die Size	10.852mm x 1.65mm
Die Thickness	457um
Min I/O pd pitch	70um
Min SEG pad pitch	27um
Min COM pad pitch	35um
Bump Height	nominal 15um

Bump Size	
Pad #	**size [um^2]**
217-607	18um x 84um
1-62, 129-190, 192-215, 609-632	26um x 60um
63-128	45um x 90um
191, 633	50um x 60um
216, 608	50um x 84um

Table 5-1 : SSD1355Z Pin Assignment Table

Pad#	Signal	X-pos	Y-pos	Pad#	Signal	X-pos	Y-pos	Pad#	Signal	X-pos	Y-pos	Pad#	Signal	X-pos	Y-pos
1	VLSS	-5078.9	-724.45	81	VDDIO	-1440.59	-709.45	161	COM49	4063.9	-724.45	241	SA8	4620.45	744
2	VLSS	-5043.9	-724.45	82	BS1	-1370.39	-709.45	162	COM48	4098.9	-724.45	242	SB8	4593.45	744
3	COM102	-5008.9	-724.45	83	VSS	-1300.59	-709.45	163	COM47	4133.9	-724.45	243	SC8	4566.45	744
4	COM103	-4973.9	-724.45	84	TE	-1209.17	-709.45	164	COM46	4168.9	-724.45	244	SA9	4539.45	744
5	COM104	-4938.9	-724.45	85	CL	-1119.53	-709.45	165	COM45	4203.9	-724.45	245	SB9	4512.45	744
6	COM105	-4903.9	-724.45	86	VSS	-1049.53	-709.45	166	COM44	4238.9	-724.45	246	SC9	4485.45	744
7	COM106	-4868.9	-724.45	87	CS#	-979.53	-709.45	167	COM43	4273.9	-724.45	247	SA10	4458.45	744
8	COM107	-4833.9	-724.45	88	RES#	-909.53	-709.45	168	COM42	4308.9	-724.45	248	SB10	4431.45	744
9	COM108	-4798.9	-724.45	89	D/C#	-839.53	-709.45	169	COM41	4343.9	-724.45	249	SC10	4404.45	744
10	COM109	-4763.9	-724.45	90	R/W# (WR#)	-699.62	-709.45	170	COM40	4378.9	-724.45	250	SA11	4377.45	744
11	COM110	-4728.9	-724.45	91	E (RD#)	-629.44	-709.45	171	COM39	4413.9	-724.45	251	SB11	4350.45	744
12	COM111	-4693.9	-724.45	92	VDDIO	-559.53	-709.45	172	COM38	4448.9	-724.45	252	SC11	4323.45	744
13	COM112	-4658.9	-724.45	93	VPP	-446.09	-709.45	173	COM37	4483.9	-724.45	253	SA12	4296.45	744
14	COM113	-4623.9	-724.45	94	VPP	-376.09	-709.45	174	COM36	4518.9	-724.45	254	SB12	4269.45	744
15	COM114	-4588.9	-724.45	95	VPP	-283.43	-709.45	175	COM35	4553.9	-724.45	255	SC12	4242.45	744
16	COM115	-4553.9	-724.45	96	VDD	-126.55	-709.45	176	COM34	4588.9	-724.45	256	SA13	4215.45	744
17	COM116	-4518.9	-724.45	97	VDD	-56.55	-709.45	177	COM33	4623.9	-724.45	257	SB13	4188.45	744
18	COM117	-4483.9	-724.45	98	VDD	56.89	-709.45	178	COM32	4658.9	-724.45	258	SC13	4161.45	744
19	COM118	-4448.9	-724.45	99	VCI	170.33	-709.45	179	COM31	4693.9	-724.45	259	SA14	4134.45	744
20	COM119	-4413.9	-724.45	100	D0	261.75	-709.45	180	COM30	4728.9	-724.45	260	SB14	4107.45	744
21	COM120	-4378.9	-724.45	101	D1	347.15	-709.45	181	COM29	4763.9	-724.45	261	SC14	4080.45	744
22	COM121	-4343.9	-724.45	102	D2	456.99	-709.45	182	COM28	4798.9	-724.45	262	SA15	4053.45	744
23	COM122	-4308.9	-724.45	103	D3	542.39	-709.45	183	COM27	4833.9	-724.45	263	SB15	4026.45	744
24	COM123	-4273.9	-724.45	104	D4	652.23	-709.45	184	COM26	4868.9	-724.45	264	SC15	3999.45	744
25	COM124	-4238.9	-724.45	105	D5	737.63	-709.45	185	COM25	4903.9	-724.45	265	SA16	3972.45	744
26	COM125	-4203.9	-724.45	106	D6	847.47	-709.45	186	COM24	4938.9	-724.45	266	SB16	3945.45	744
27	COM126	-4168.9	-724.45	107	D7	932.87	-709.45	187	COM23	4973.9	-724.45	267	SC16	3918.45	744
28	COM127	-4133.9	-724.45	108	D8	1042.71	-709.45	188	COM22	5008.9	-724.45	268	SA17	3891.45	744
29	COM128	-4098.9	-724.45	109	D9	1128.11	-709.45	189	VLSS	5043.9	-724.45	269	SB17	3864.45	744
30	COM129	-4063.9	-724.45	110	D10	1237.95	-709.45	190	VLSS	5078.9	-724.45	270	SC17	3837.45	744
31	COM130	-4028.9	-724.45	111	D11	1323.35	-709.45	191	VLSS	5325.45	-742.15	271	SA18	3810.45	744
32	COM131	-3993.9	-724.45	112	D12	1433.19	-709.45	192	COM21	5325.45	-695.15	272	SB18	3783.45	744
33	COM132	-3958.9	-724.45	113	D13	1518.59	-709.45	193	COM20	5325.45	-660.15	273	SC18	3756.45	744
34	COM133	-3923.9	-724.45	114	D14	1628.43	-709.45	194	COM19	5325.45	-625.15	274	SA19	3729.45	744
35	COM134	-3888.9	-724.45	115	D15	1713.83	-709.45	195	COM18	5325.45	-590.15	275	SB19	3702.45	744
36	COM135	-3853.9	-724.45	116	D16	1823.67	-709.45	196	COM17	5325.45	-555.15	276	SC19	3675.45	744
37	COM136	-3818.9	-724.45	117	D17	1909.07	-709.45	197	COM16	5325.45	-520.15	277	SA20	3648.45	744
38	COM137	-3783.9	-724.45	118	VSS	2000.49	-709.45	198	COM15	5325.45	-485.15	278	SB20	3621.45	744
39	COM138	-3748.9	-724.45	119	BGGND	2070.49	-709.45	199	COM14	5325.45	-450.15	279	SC20	3594.45	744
40	COM139	-3713.9	-724.45	120	CLS	2140.49	-709.45	200	COM13	5325.45	-415.15	280	SA21	3567.45	744
41	COM140	-3678.9	-724.45	121	VCI	2210.49	-709.45	201	COM12	5325.45	-380.15	281	SB21	3540.45	744
42	COM141	-3643.9	-724.45	122	VDDIO	2367.37	-709.45	202	COM11	5325.45	-345.15	282	SC21	3513.45	744
43	COM142	-3608.9	-724.45	123	VDD	2437.37	-709.45	203	COM10	5325.45	-310.15	283	SA22	3486.45	744
44	COM143	-3573.9	-724.45	124	IREF	2550.81	-709.45	204	COM9	5325.45	-275.15	284	SB22	3459.45	744
45	COM144	-3538.9	-724.45	125	VCOMH	2620.81	-709.45	205	COM8	5325.45	-240.15	285	SC22	3432.45	744
46	COM145	-3503.9	-724.45	126	VCOMH	2690.81	-709.45	206	COM7	5325.45	-205.15	286	SA23	3405.45	744
47	COM146	-3468.9	-724.45	127	VCC	2792.29	-709.45	207	COM6	5325.45	-170.15	287	SB23	3378.45	744
48	COM147	-3433.9	-724.45	128	VCC	2862.29	-709.45	208	COM5	5325.45	-135.15	288	SC23	3351.45	744
49	COM148	-3398.9	-724.45	129	VLSS	2943.9	-724.45	209	COM4	5325.45	-100.15	289	SA24	3324.45	744
50	COM149	-3363.9	-724.45	130	VLSS	2978.9	-724.45	210	COM3	5325.45	-65.15	290	SB24	3297.45	744
51	COM150	-3328.9	-724.45	131	COM79	3013.9	-724.45	211	COM2	5325.45	-30.15	291	SC24	3270.45	744
52	COM151	-3293.9	-724.45	132	COM78	3048.9	-724.45	212	COM1	5325.45	4.85	292	SA25	3243.45	744
53	COM152	-3258.9	-724.45	133	COM77	3083.9	-724.45	213	COM0	5325.45	39.85	293	SB25	3216.45	744
54	COM153	-3223.9	-724.45	134	COM76	3118.9	-724.45	214	VLSS	5325.45	74.85	294	SC25	3189.45	744
55	COM154	-3188.9	-724.45	135	COM75	3153.9	-724.45	215	VLSS	5325.45	109.85	295	SA26	3162.45	744
56	COM155	-3153.9	-724.45	136	COM74	3188.9	-724.45	216	VCC	5337.26	744	296	SB26	3135.45	744
57	COM156	-3118.9	-724.45	137	COM73	3223.9	-724.45	217	SA0	5268.45	744	297	SC26	3108.45	744
58	COM157	-3083.9	-724.45	138	COM72	3258.9	-724.45	218	SB0	5241.45	744	298	SA27	3081.45	744
59	COM158	-3048.9	-724.45	139	COM71	3293.9	-724.45	219	SC0	5214.45	744	299	SB27	3054.45	744
60	COM159	-3013.9	-724.45	140	COM70	3328.9	-724.45	220	SA1	5187.45	744	300	SC27	3027.45	744
61	VLSS	-2978.9	-724.45	141	COM69	3363.9	-724.45	221	SB1	5160.45	744	301	SA28	3000.45	744
62	VLSS	-2943.9	-724.45	142	COM68	3398.9	-724.45	222	SC1	5133.45	744	302	SB28	2973.45	744
63	VCC	-2876.99	-709.45	143	COM67	3433.9	-724.45	223	SA2	5106.45	744	303	SC28	2946.45	744
64	VCC	-2806.99	-709.45	144	COM66	3468.9	-724.45	224	SB2	5079.45	744	304	SA29	2919.45	744
65	VCOMH	-2705.51	-709.45	145	COM65	3503.9	-724.45	225	SC2	5052.45	744	305	SB29	2892.45	744
66	VCOMH	-2635.51	-709.45	146	COM64	3538.9	-724.45	226	SA3	5025.45	744	306	SC29	2865.45	744
67	VSS	-2565.51	-709.45	147	COM63	3573.9	-724.45	227	SB3	4998.45	744	307	SA30	2838.45	744
68	VSS	-2495.51	-709.45	148	COM62	3608.9	-724.45	228	SC3	4971.45	744	308	SB30	2811.45	744
69	VSL	-2425.51	-709.45	149	COM61	3643.9	-724.45	229	SA4	4944.45	744	309	SC30	2784.45	744
70	VSL	-2355.51	-709.45	150	COM60	3678.9	-724.45	230	SB4	4917.45	744	310	SA31	2757.45	744
71	VCI	-2285.51	-709.45	151	COM59	3713.9	-724.45	231	SC4	4890.45	744	311	SB31	2730.45	744
72	VCI	-2215.51	-709.45	152	COM58	3748.9	-724.45	232	SA5	4863.45	744	312	SC31	2703.45	744
73	VDDIO	-2102.07	-709.45	153	COM57	3783.9	-724.45	233	SB5	4836.45	744	313	SA32	2676.45	744
74	VDDIO	-2032.07	-709.45	154	COM56	3818.9	-724.45	234	SC5	4809.45	744	314	SB32	2649.45	744
75	VDD	-1918.63	-709.45	155	COM55	3853.9	-724.45	235	SA6	4782.45	744	315	SC32	2622.45	744
76	VLSS	-1848.63	-709.45	156	COM54	3888.9	-724.45	236	SB6	4755.45	744	316	SA33	2595.45	744
77	GPIO0	-1757.21	-709.45	157	COM53	3923.9	-724.45	237	SC6	4728.45	744	317	SB33	2568.45	744
78	GPIO1	-1671.81	-709.45	158	COM52	3958.9	-724.45	238	SA7	4701.45	744	318	SC33	2541.45	744
79	VSS	-1580.59	-709.45	159	COM51	3993.9	-724.45	239	SB7	4674.45	744	319	SA34	2514.45	744
80	BS0	-1510.39	-709.45	160	COM50	4028.9	-724.45	240	SC7	4647.45	744	320	SB34	2487.45	744

Pad#	Signal	X-pos	Y-pos	Pad#	Signal	X-pos	Y-pos	Pad#	Signal	X-pos	Y-pos	Pad#	Signal	X-pos	Y-pos
321	SC34	2460.45	744	401	SB61	300.45	744	481	SC85	-1859.55	744	561	SB112	-4019.55	744
322	SA35	2433.45	744	402	SC61	273.45	744	482	SA86	-1886.55	744	562	SC112	-4046.55	744
323	SB35	2406.45	744	403	SA62	246.45	744	483	SB86	-1913.55	744	563	SA113	-4073.55	744
324	SC35	2379.45	744	404	SB62	219.45	744	484	SC86	-1940.55	744	564	SB113	-4100.55	744
325	SA36	2352.45	744	405	SC62	192.45	744	485	SA87	-1967.55	744	565	SC113	-4127.55	744
326	SB36	2325.45	744	406	SA63	165.45	744	486	SB87	-1994.55	744	566	SA114	-4154.55	744
327	SC36	2298.45	744	407	SB63	138.45	744	487	SC87	-2021.55	744	567	SB114	-4181.55	744
328	SA37	2271.45	744	408	SC63	111.45	744	488	SA88	-2048.55	744	568	SC114	-4208.55	744
329	SB37	2244.45	744	409	SA64	84.45	744	489	SB88	-2075.55	744	569	SA115	-4235.55	744
330	SC37	2217.45	744	410	SB64	57.45	744	490	SC88	-2102.55	744	570	SB115	-4262.55	744
331	SA38	2190.45	744	411	SC64	30.45	744	491	SA89	-2129.55	744	571	SC115	-4289.55	744
332	SB38	2163.45	744	412	SA65	3.45	744	492	SB89	-2156.55	744	572	SA116	-4316.55	744
333	SC38	2136.45	744	413	SB65	-23.55	744	493	SC89	-2183.55	744	573	SB116	-4343.55	744
334	SA39	2109.45	744	414	SC65	-50.55	744	494	SA90	-2210.55	744	574	SC116	-4370.55	744
335	SB39	2082.45	744	415	SA66	-77.55	744	495	SB90	-2237.55	744	575	SA117	-4397.55	744
336	SC39	2055.45	744	416	SB66	-104.55	744	496	SC90	-2264.55	744	576	SB117	-4424.55	744
337	SA40	2028.45	744	417	SC66	-131.55	744	497	SA91	-2291.55	744	577	SC117	-4451.55	744
338	SB40	2001.45	744	418	SA67	-158.55	744	498	SB91	-2318.55	744	578	SA118	-4478.55	744
339	SC40	1974.45	744	419	SB67	-185.55	744	499	SC91	-2345.55	744	579	SB118	-4505.55	744
340	SA41	1947.45	744	420	SC67	-212.55	744	500	SA92	-2372.55	744	580	SC118	-4532.55	744
341	SB41	1920.45	744	421	SA68	-239.55	744	501	SB92	-2399.55	744	581	SA119	-4559.55	744
342	SC41	1893.45	744	422	SB68	-266.55	744	502	SC92	-2426.55	744	582	SB119	-4586.55	744
343	SA42	1866.45	744	423	SC68	-293.55	744	503	SA93	-2453.55	744	583	SC119	-4613.55	744
344	SB42	1839.45	744	424	SA69	-320.55	744	504	SB93	-2480.55	744	584	SA120	-4640.55	744
345	SC42	1812.45	744	425	SB69	-347.55	744	505	SC93	-2507.55	744	585	SB120	-4667.55	744
346	SA43	1785.45	744	426	SC69	-374.55	744	506	SA94	-2534.55	744	586	SC120	-4694.55	744
347	SB43	1758.45	744	427	SA70	-401.55	744	507	SB94	-2561.55	744	587	SA121	-4721.55	744
348	SC43	1731.45	744	428	SB70	-428.55	744	508	SC94	-2588.55	744	588	SB121	-4748.55	744
349	SA44	1704.45	744	429	SC70	-455.55	744	509	SA95	-2615.55	744	589	SC121	-4775.55	744
350	SB44	1677.45	744	430	SA71	-482.55	744	510	SB95	-2642.55	744	590	SA122	-4802.55	744
351	SC44	1650.45	744	431	SB71	-509.55	744	511	SC95	-2669.55	744	591	SB122	-4829.55	744
352	SA45	1623.45	744	432	SC71	-536.55	744	512	SA96	-2696.55	744	592	SC122	-4856.55	744
353	SB45	1596.45	744	433	SA72	-563.55	744	513	SB96	-2723.55	744	593	SA123	-4883.55	744
354	SC45	1569.45	744	434	SB72	-590.55	744	514	SC96	-2750.55	744	594	SB123	-4910.55	744
355	SA46	1542.45	744	435	SC72	-617.55	744	515	SA97	-2777.55	744	595	SC123	-4937.55	744
356	SB46	1515.45	744	436	SA73	-644.55	744	516	SB97	-2804.55	744	596	SA124	-4964.55	744
357	SC46	1488.45	744	437	SB73	-671.55	744	517	SC97	-2831.55	744	597	SB124	-4991.55	744
358	SA47	1461.45	744	438	SC73	-698.55	744	518	SA98	-2858.55	744	598	SC124	-5018.55	744
359	SB47	1434.45	744	439	VSS	-725.55	744	519	SB98	-2885.55	744	599	SA125	-5045.55	744
360	SC47	1407.45	744	440	VSS	-752.55	744	520	SC98	-2912.55	744	600	SB125	-5072.55	744
361	SA48	1380.45	744	441	VSS	-779.55	744	521	SA99	-2939.55	744	601	SC125	-5099.55	744
362	SB48	1353.45	744	442	VSS	-806.55	744	522	SB99	-2966.55	744	602	SA126	-5126.55	744
363	SC48	1326.45	744	443	VSS	-833.55	744	523	SC99	-2993.55	744	603	SB126	-5153.55	744
364	SA49	1299.45	744	444	VSS	-860.55	744	524	SA100	-3020.55	744	604	SC126	-5180.55	744
365	SB49	1272.45	744	445	VSS	-887.55	744	525	SB100	-3047.55	744	605	SA127	-5207.55	744
366	SC49	1245.45	744	446	SA74	-914.55	744	526	SC100	-3074.55	744	606	SB127	-5234.55	744
367	SA50	1218.45	744	447	SB74	-941.55	744	527	SA101	-3101.55	744	607	SC127	-5261.55	744
368	SB50	1191.45	744	448	SC74	-968.55	744	528	SB101	-3128.55	744	608	VCC	-5337.26	744
369	SC50	1164.45	744	449	SA75	-995.55	744	529	SC101	-3155.55	744	609	VLSS	-5325.45	109.85
370	SA51	1137.45	744	450	SB75	-1022.55	744	530	SA102	-3182.55	744	610	VLSS	-5325.45	74.85
371	SB51	1110.45	744	451	SC75	-1049.55	744	531	SB102	-3209.55	744	611	COM80	-5325.45	39.85
372	SC51	1083.45	744	452	SA76	-1076.55	744	532	SC102	-3236.55	744	612	COM81	-5325.45	4.85
373	SA52	1056.45	744	453	SB76	-1103.55	744	533	SA103	-3263.55	744	613	COM82	-5325.45	-30.15
374	SB52	1029.45	744	454	SC76	-1130.55	744	534	SB103	-3290.55	744	614	COM83	-5325.45	-65.15
375	SC52	1002.45	744	455	SA77	-1157.55	744	535	SC103	-3317.55	744	615	COM84	-5325.45	-100.15
376	SA53	975.45	744	456	SB77	-1184.55	744	536	SA104	-3344.55	744	616	COM85	-5325.45	-135.15
377	SB53	948.45	744	457	SC77	-1211.55	744	537	SB104	-3371.55	744	617	COM86	-5325.45	-170.15
378	SC53	921.45	744	458	SA78	-1238.55	744	538	SC104	-3398.55	744	618	COM87	-5325.45	-205.15
379	SA54	894.45	744	459	SB78	-1265.55	744	539	SA105	-3425.55	744	619	COM88	-5325.45	-240.15
380	SB54	867.45	744	460	SC78	-1292.55	744	540	SB105	-3452.55	744	620	COM89	-5325.45	-275.15
381	SC54	840.45	744	461	SA79	-1319.55	744	541	SC105	-3479.55	744	621	COM90	-5325.45	-310.15
382	SA55	813.45	744	462	SB79	-1346.55	744	542	SA106	-3506.55	744	622	COM91	-5325.45	-345.15
383	SB55	786.45	744	463	SC79	-1373.55	744	543	SB106	-3533.55	744	623	COM92	-5325.45	-380.15
384	SC55	759.45	744	464	SA80	-1400.55	744	544	SC106	-3560.55	744	624	COM93	-5325.45	-415.15
385	SA56	732.45	744	465	SB80	-1427.55	744	545	SA107	-3587.55	744	625	COM94	-5325.45	-450.15
386	SB56	705.45	744	466	SC80	-1454.55	744	546	SB107	-3614.55	744	626	COM95	-5325.45	-485.15
387	SC56	678.45	744	467	SA81	-1481.55	744	547	SC107	-3641.55	744	627	COM96	-5325.45	-520.15
388	SA57	651.45	744	468	SB81	-1508.55	744	548	SA108	-3668.55	744	628	COM97	-5325.45	-555.15
389	SB57	624.45	744	469	SC81	-1535.55	744	549	SB108	-3695.55	744	629	COM98	-5325.45	-590.15
390	SC57	597.45	744	470	SA82	-1562.55	744	550	SC108	-3722.55	744	630	COM99	-5325.45	-625.15
391	SA58	570.45	744	471	SB82	-1589.55	744	551	SA109	-3749.55	744	631	COM100	-5325.45	-660.15
392	SB58	543.45	744	472	SC82	-1616.55	744	552	SB109	-3776.55	744	632	COM101	-5325.45	-695.15
393	SC58	516.45	744	473	SA83	-1643.55	744	553	SC109	-3803.55	744	633	VLSS	-5325.45	-742.15
394	SA59	489.45	744	474	SB83	-1670.55	744	554	SA110	-3830.55	744				
395	SB59	462.45	744	475	SC83	-1697.55	744	555	SB110	-3857.55	744				
396	SC59	435.45	744	476	SA84	-1724.55	744	556	SC110	-3884.55	744				
397	SA60	408.45	744	477	SB84	-1751.55	744	557	SA111	-3911.55	744				
398	SB60	381.45	744	478	SC84	-1778.55	744	558	SB111	-3938.55	744				
399	SC60	354.45	744	479	SA85	-1805.55	744	559	SC111	-3965.55	744				
400	SA61	327.45	744	480	SB85	-1832.55	744	560	SA112	-3992.55	744				

6 PIN ARRANGEMENT

6.1 SSD1355U2R1 Pin Assignment

Figure 6-1: SSD1355U2R1 Pin Assignment

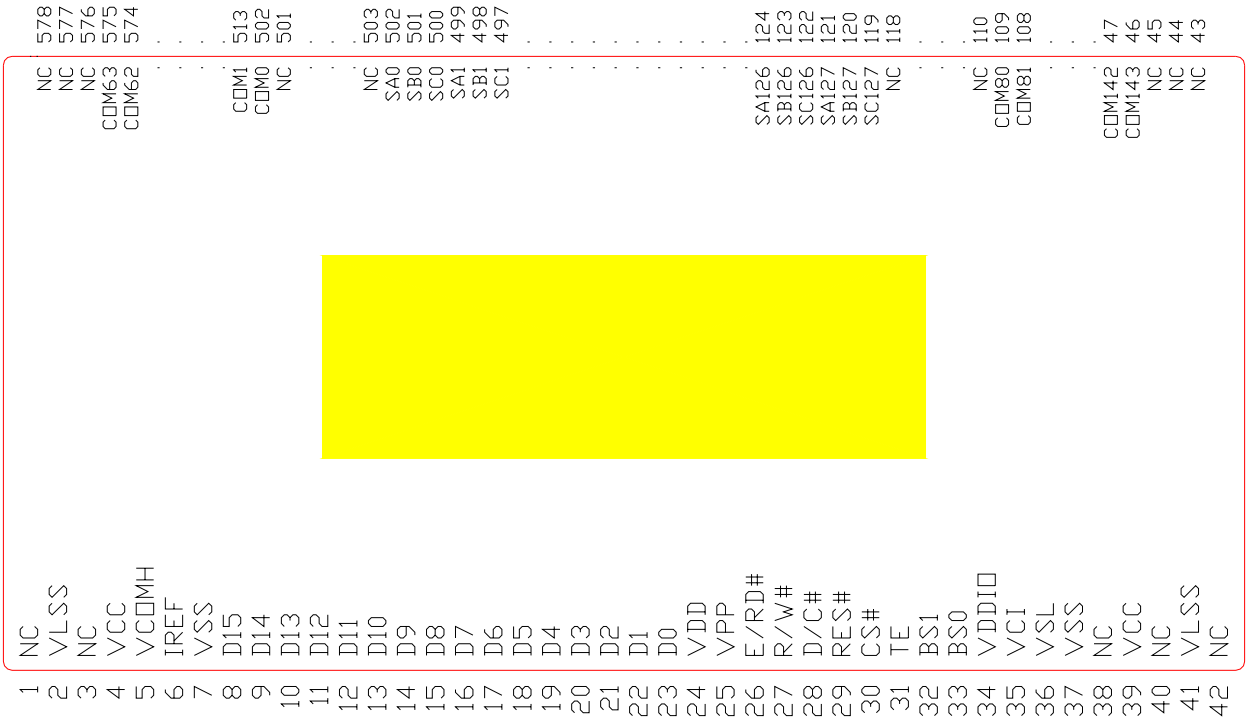


Table 6-1 : SSD1355U2R1 Pin Assignment Table

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	NC	81	COM92	161	SC113	241	SA87
2	VLSS	82	COM91	162	SB113	242	SC86
3	NC	83	COM90	163	SA113	243	SB86
4	VCC	84	COM89	164	SC112	244	SA86
5	VCOMH	85	COM88	165	SB112	245	SC85
6	IREF	86	COM87	166	SA112	246	SB85
7	VSS	87	COM86	167	SC111	247	SA85
8	D15	88	COM85	168	SB111	248	SC84
9	D14	89	COM84	169	SA111	249	SB84
10	D13	90	COM83	170	SC110	250	SA84
11	D12	91	COM82	171	SB110	251	SC83
12	D11	92	COM81	172	SA110	252	SB83
13	D10	93	COM80	173	SC109	253	SA83
14	D9	94	COM79	174	SB109	254	SC82
15	D8	95	COM78	175	SA109	255	SB82
16	D7	96	COM77	176	SC108	256	SA82
17	D6	97	COM76	177	SB108	257	SC81
18	D5	98	COM75	178	SA108	258	SB81
19	D4	99	COM74	179	SC107	259	SA81
20	D3	100	COM73	180	SB107	260	SC80
21	D2	101	COM72	181	SA107	261	SB80
22	D1	102	COM71	182	SC106	262	SA80
23	D0	103	COM70	183	SB106	263	SC79
24	VDD	104	COM69	184	SA106	264	SB79
25	VPP	105	COM68	185	SC105	265	SA79
26	E/RD#	106	COM67	186	SB105	266	SC78
27	R/W#	107	COM66	187	SA105	267	SB78
28	D/C#	108	COM65	188	SC104	268	SA78
29	RES#	109	COM64	189	SB104	269	SC77
30	CS#	110	NC	190	SA104	270	SB77
31	TE	111	NC	191	SC103	271	SA77
32	BS1	112	NC	192	SB103	272	SC76
33	BS0	113	NC	193	SA103	273	SB76
34	VDDIO	114	NC	194	SC102	274	SA76
35	VCI	115	NC	195	SB102	275	SC75
36	VSL	116	NC	196	SA102	276	SB75
37	VSS	117	NC	197	SC101	277	SA75
38	NC	118	NC	198	SB101	278	SC74
39	VCC	119	SC127	199	SA101	279	SB74
40	NC	120	SB127	200	SC100	280	SA74
41	VLSS	121	SA127	201	SB100	281	SC73
42	NC	122	SC126	202	SA100	282	SB73
43	NC	123	SB126	203	SC99	283	SA73
44	NC	124	SA126	204	SB99	284	SC72
45	NC	125	SC125	205	SA99	285	SB72
46	COM127	126	SB125	206	SC98	286	SA72
47	COM126	127	SA125	207	SB98	287	SC71
48	COM125	128	SC124	208	SA98	288	SB71
49	COM124	129	SB124	209	SC97	289	SA71
50	COM123	130	SA124	210	SB97	290	SC70
51	COM122	131	SC123	211	SA97	291	SB70
52	COM121	132	SB123	212	SC96	292	SA70
53	COM120	133	SA123	213	SB96	293	SC69
54	COM119	134	SC122	214	SA96	294	SB69
55	COM118	135	SB122	215	SC95	295	SA69
56	COM117	136	SA122	216	SB95	296	SC68
57	COM116	137	SC121	217	SA95	297	SB68
58	COM115	138	SB121	218	SC94	298	SA68
59	COM114	139	SA121	219	SB94	299	SC67
60	COM113	140	SC120	220	SA94	300	SB67
61	COM112	141	SB120	221	SC93	301	SA67
62	COM111	142	SA120	222	SB93	302	SC66
63	COM110	143	SC119	223	SA93	303	SB66
64	COM109	144	SB119	224	SC92	304	SA66
65	COM108	145	SA119	225	SB92	305	SC65
66	COM107	146	SC118	226	SA92	306	SB65
67	COM106	147	SB118	227	SC91	307	SA65
68	COM105	148	SA118	228	SB91	308	SC64
69	COM104	149	SC117	229	SA91	309	SB64
70	COM103	150	SB117	230	SC90	310	SA64
71	COM102	151	SA117	231	SB90	311	SC63
72	COM101	152	SC116	232	SA90	312	SB63
73	COM100	153	SB116	233	SC89	313	SA63
74	COM99	154	SA116	234	SB89	314	SC62
75	COM98	155	SC115	235	SA89	315	SB62
76	COM97	156	SB115	236	SC88	316	SA62
77	COM96	157	SA115	237	SB88	317	SC61
78	COM95	158	SC114	238	SA88	318	SB61
79	COM94	159	SB114	239	SC87	319	SA61
80	COM93	160	SA114	240	SB87	320	SC60

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
321	SB60	401	SC33	481	SA7	561	COM49
322	SA60	402	SB33	482	SC6	562	COM50
323	SC59	403	SA33	483	SB6	563	COM51
324	SB59	404	SC32	484	SA6	564	COM52
325	SA59	405	SB32	485	SC5	565	COM53
326	SC58	406	SA32	486	SB5	566	COM54
327	SB58	407	SC31	487	SA5	567	COM55
328	SA58	408	SB31	488	SC4	568	COM56
329	SC57	409	SA31	489	SB4	569	COM57
330	SB57	410	SC30	490	SA4	570	COM58
331	SA57	411	SB30	491	SC3	571	COM59
332	SC56	412	SA30	492	SB3	572	COM60
333	SB56	413	SC29	493	SA3	573	COM61
334	SA56	414	SB29	494	SC2	574	COM62
335	SC55	415	SA29	495	SB2	575	COM63
336	SB55	416	SC28	496	SA2	576	NC
337	SA55	417	SB28	497	SC1	577	NC
338	SC54	418	SA28	498	SB1	578	NC
339	SB54	419	SC27	499	SA1		
340	SA54	420	SB27	500	SC0		
341	SC53	421	SA27	501	SB0		
342	SB53	422	SC26	502	SA0		
343	SA53	423	SB26	503	NC		
344	SC52	424	SA26	504	NC		
345	SB52	425	SC25	505	NC		
346	SA52	426	SB25	506	NC		
347	SC51	427	SA25	507	NC		
348	SB51	428	SC24	508	NC		
349	SA51	429	SB24	509	NC		
350	SC50	430	SA24	510	NC		
351	SB50	431	SC23	511	NC		
352	SA50	432	SB23	512	COM0		
353	SC49	433	SA23	513	COM1		
354	SB49	434	SC22	514	COM2		
355	SA49	435	SB22	515	COM3		
356	SC48	436	SA22	516	COM4		
357	SB48	437	SC21	517	COM5		
358	SA48	438	SB21	518	COM6		
359	SC47	439	SA21	519	COM7		
360	SB47	440	SC20	520	COM8		
361	SA47	441	SB20	521	COM9		
362	SC46	442	SA20	522	COM10		
363	SB46	443	SC19	523	COM11		
364	SB46	444	SB19	524	COM12		
365	SC45	445	SA19	525	COM13		
366	SB45	446	SC18	526	COM14		
367	SA45	447	SB18	527	COM15		
368	SC44	448	SA18	528	COM16		
369	SB44	449	SC17	529	COM17		
370	SA44	450	SB17	530	COM18		
371	SC43	451	SA17	531	COM19		
372	SB43	452	SC16	532	COM20		
373	SA43	453	SB16	533	COM21		
374	SC42	454	SA16	534	COM22		
375	SB42	455	SC15	535	COM23		
376	SA42	456	SB15	536	COM24		
377	SC41	457	SA15	537	COM25		
378	SB41	458	SC14	538	COM26		
379	SA41	459	SB14	539	COM27		
380	SC40	460	SA14	540	COM28		
381	SB40	461	SC13	541	COM29		
382	SA40	462	SB13	542	COM30		
383	SC39	463	SA13	543	COM31		
384	SB39	464	SC12	544	COM32		
385	SA39	465	SB12	545	COM33		
386	SC38	466	SA12	546	COM34		
387	SB38	467	SC11	547	COM35		
388	SA38	468	SB11	548	COM36		
389	SC37	469	SA11	549	COM37		
390	SB37	470	SC10	550	COM38		
391	SA37	471	SB10	551	COM39		
392	SC36	472	SA10	552	COM40		
393	SB36	473	SC9	553	COM41		
394	SA36	474	SB9	554	COM42		
395	SC35	475	SA9	555	COM43		
396	SB35	476	SC8	556	COM44		
397	SA35	477	SB8	557	COM45		
398	SC34	478	SA8	558	COM46		
399	SB34	479	SC7	559	COM47		
400	SA34	480	SB7	560	COM48		

6.2 SSD1355U3R1 Pin Assignment

Figure 6-2: SSD1355U3R1 Pin Assignment

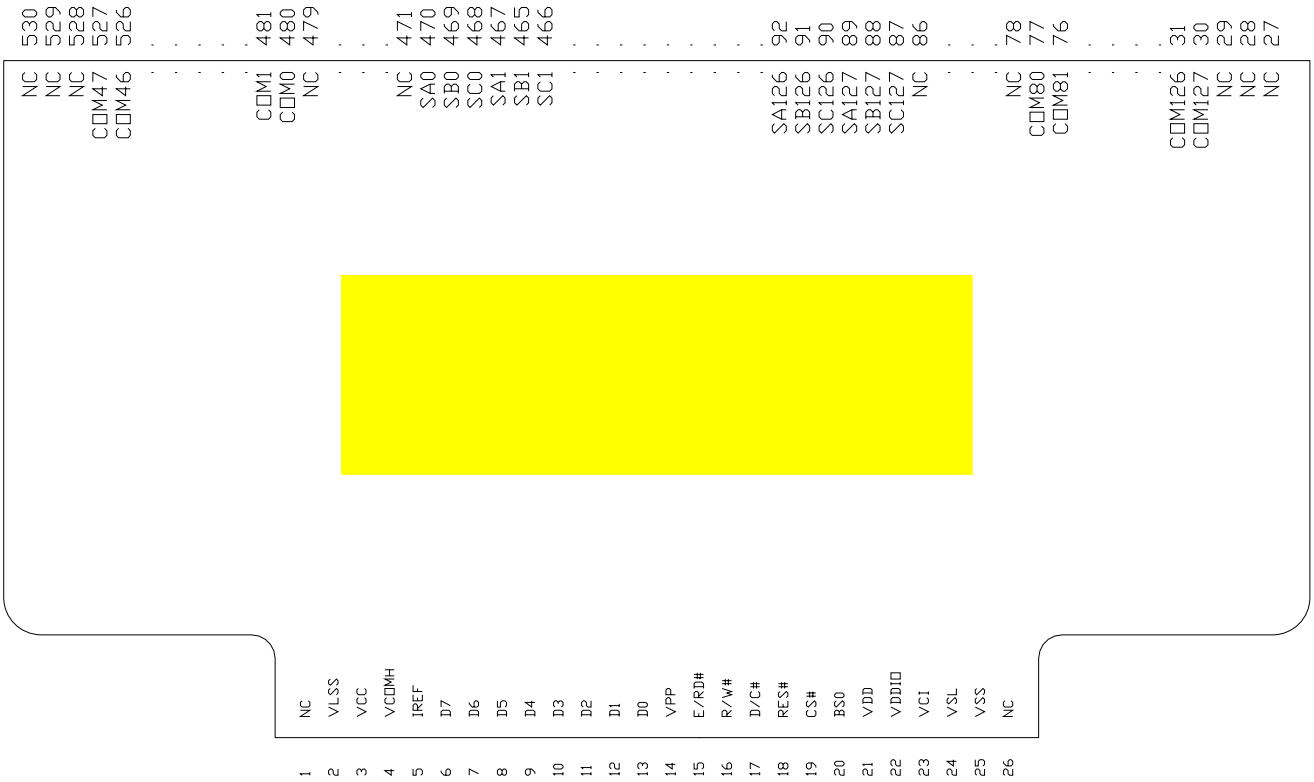


Table 6-2: SSD1355U3R1 Pin Assignment Table

Pin No.	Pin Name	Pin No.	Name	Pin No.	Pin Name	Pin No.	Name
1	NC	81	NC	161	SA103	241	SB76
2	VLSS	82	NC	162	SC102	242	SA76
3	VCC	83	NC	163	SB102	243	SC75
4	VCOMH	84	NC	164	SA102	244	SB75
5	IREF	85	NC	165	SC101	245	SA75
6	D7	86	NC	166	SB101	246	SC74
7	D6	87	SC127	167	SA101	247	SB74
8	D5	88	SB127	168	SC100	248	SA74
9	D4	89	SA127	169	SB100	249	SC73
10	D3	90	SC126	170	SA100	250	SB73
11	D2	91	SB126	171	SC99	251	SA73
12	D1	92	SA126	172	SB99	252	SC72
13	D0	93	SC125	173	SA99	253	SB72
14	VPP	94	SB125	174	SC98	254	SA72
15	E/RD#	95	SA125	175	SB98	255	SC71
16	R/W#	96	SC124	176	SA98	256	SB71
17	D/C#	97	SB124	177	SC97	257	SA71
18	RES#	98	SA124	178	SB97	258	SC70
19	CS#	99	SC123	179	SA97	259	SB70
20	BS0	100	SB123	180	SC96	260	SA70
21	VDD	101	SA123	181	SB96	261	SC69
22	VDDIO	102	SC122	182	SA96	262	SB69
23	VCI	103	SB122	183	SC95	263	SA69
24	VSL	104	SA122	184	SB95	264	SC68
25	VSS	105	SC121	185	SA95	265	SB68
26	NC	106	SB121	186	SC94	266	SA68
27	NC	107	SA121	187	SB94	267	SC67
28	NC	108	SC120	188	SA94	268	SB67
29	NC	109	SB120	189	SC93	269	SA67
30	COM95	110	SA120	190	SB93	270	SC66
31	COM94	111	SC119	191	SA93	271	SB66
32	COM93	112	SB119	192	SC92	272	SA66
33	COM92	113	SA119	193	SB92	273	SC65
34	COM91	114	SC118	194	SA92	274	SB65
35	COM90	115	SB118	195	SC91	275	SA65
36	COM89	116	SA118	196	SB91	276	SC64
37	COM88	117	SC117	197	SA91	277	SB64
38	COM87	118	SB117	198	SC90	278	SA64
39	COM86	119	SA117	199	SB90	279	SC63
40	COM85	120	SC116	200	SA90	280	SB63
41	COM84	121	SB116	201	SC89	281	SA63
42	COM83	122	SA116	202	SB89	282	SC62
43	COM82	123	SC115	203	SA89	283	SB62
44	COM81	124	SB115	204	SC88	284	SA62
45	COM80	125	SA115	205	SB88	285	SC61
46	COM79	126	SC114	206	SA88	286	SB61
47	COM78	127	SB114	207	SC87	287	SA61
48	COM77	128	SA114	208	SB87	288	SC60
49	COM76	129	SC113	209	SA87	289	SB60
50	COM75	130	SB113	210	SC86	290	SA60
51	COM74	131	SA113	211	SB86	291	SC59
52	COM73	132	SC112	212	SA86	292	SB59
53	COM72	133	SB112	213	SC85	293	SA59
54	COM71	134	SA112	214	SB85	294	SC58
55	COM70	135	SC111	215	SA85	295	SB58
56	COM69	136	SB111	216	SC84	296	SA58
57	COM68	137	SA111	217	SB84	297	SC57
58	COM67	138	SC110	218	SA84	298	SB57
59	COM66	139	SB110	219	SC83	299	SA57
60	COM65	140	SA110	220	SB83	300	SC56
61	COM64	141	SC109	221	SA83	301	SB56
62	COM63	142	SB109	222	SC82	302	SA56
63	COM62	143	SA109	223	SB82	303	SC55
64	COM61	144	SC108	224	SA82	304	SB55
65	COM60	145	SB108	225	SC81	305	SA55
66	COM59	146	SA108	226	SB81	306	SC54
67	COM58	147	SC107	227	SA81	307	SB54
68	COM57	148	SB107	228	SC80	308	SA54
69	COM56	149	SA107	229	SB80	309	SC53
70	COM55	150	SC106	230	SA80	310	SB53
71	COM54	151	SB106	231	SC79	311	SA53
72	COM53	152	SA106	232	SB79	312	SC52
73	COM52	153	SC105	233	SA79	313	SB52
74	COM51	154	SB105	234	SC78	314	SA52
75	COM50	155	SA105	235	SB78	315	SC51
76	COM49	156	SC104	236	SA78	316	SB51
77	COM48	157	SB104	237	SC77	317	SA51
78	NC	158	SA104	238	SB77	318	SC50
79	NC	159	SC103	239	SA77	319	SB50
80	NC	160	SB103	240	SC76	320	SA50

Pin No.	Pin Name	Pin No.	Name	Pin No.	Pin Name
321	SC49	401	SA23	481	COM1
322	SB49	402	SC22	482	COM2
323	SA49	403	SB22	483	COM3
324	SC48	404	SA22	484	COM4
325	SB48	405	SC21	485	COM5
326	SA48	406	SB21	486	COM6
327	SC47	407	SA21	487	COM7
328	SB47	408	SC20	488	COM8
329	SA47	409	SB20	489	COM9
330	SC46	410	SA20	490	COM10
331	SB46	411	SC19	491	COM11
332	SB46	412	SB19	492	COM12
333	SC45	413	SA19	493	COM13
334	SB45	414	SC18	494	COM14
335	SA45	415	SB18	495	COM15
336	SC44	416	SA18	496	COM16
337	SB44	417	SC17	497	COM17
338	SA44	418	SB17	498	COM18
339	SC43	419	SA17	499	COM19
340	SB43	420	SC16	500	COM20
341	SA43	421	SB16	501	COM21
342	SC42	422	SA16	502	COM22
343	SB42	423	SC15	503	COM23
344	SA42	424	SB15	504	COM24
345	SC41	425	SA15	505	COM25
346	SB41	426	SC14	506	COM26
347	SA41	427	SB14	507	COM27
348	SC40	428	SA14	508	COM28
349	SB40	429	SC13	509	COM29
350	SA40	430	SB13	510	COM30
351	SC39	431	SA13	511	COM31
352	SB39	432	SC12	512	COM32
353	SA39	433	SB12	513	COM33
354	SC38	434	SA12	514	COM34
355	SB38	435	SC11	515	COM35
356	SA38	436	SB11	516	COM36
357	SC37	437	SA11	517	COM37
358	SB37	438	SC10	518	COM38
359	SA37	439	SB10	519	COM39
360	SC36	440	SA10	520	COM40
361	SB36	441	SC9	521	COM41
362	SA36	442	SB9	522	COM42
363	SC35	443	SA9	523	COM43
364	SB35	444	SC8	524	COM44
365	SA35	445	SB8	525	COM45
366	SC34	446	SA8	526	COM46
367	SB34	447	SC7	527	COM47
368	SA34	448	SB7	528	NC
369	SC33	449	SA7	529	NC
370	SB33	450	SC6	530	NC
371	SA33	451	SB6		
372	SC32	452	SA6		
373	SB32	453	SC5		
374	SA32	454	SB5		
375	SC31	455	SA5		
376	SB31	456	SC4		
377	SA31	457	SB4		
378	SC30	458	SA4		
379	SB30	459	SC3		
380	SA30	460	SB3		
381	SC29	461	SA3		
382	SB29	462	SC2		
383	SA29	463	SB2		
384	SC28	464	SA2		
385	SB28	465	SC1		
386	SA28	466	SB1		
387	SC27	467	SA1		
388	SB27	468	SC0		
389	SA27	469	SB0		
390	SC26	470	SA0		
391	SB26	471	NC		
392	SA26	472	NC		
393	SC25	473	NC		
394	SB25	474	NC		
395	SA25	475	NC		
396	SC24	476	NC		
397	SB24	477	NC		
398	SA24	478	NC		
399	SC23	479	NC		
400	SB23	480	COM0		

6.3 SSD1355U6R1 Pin Assignment

Figure 6-3: SSD1355U6R1 Pin Assignment

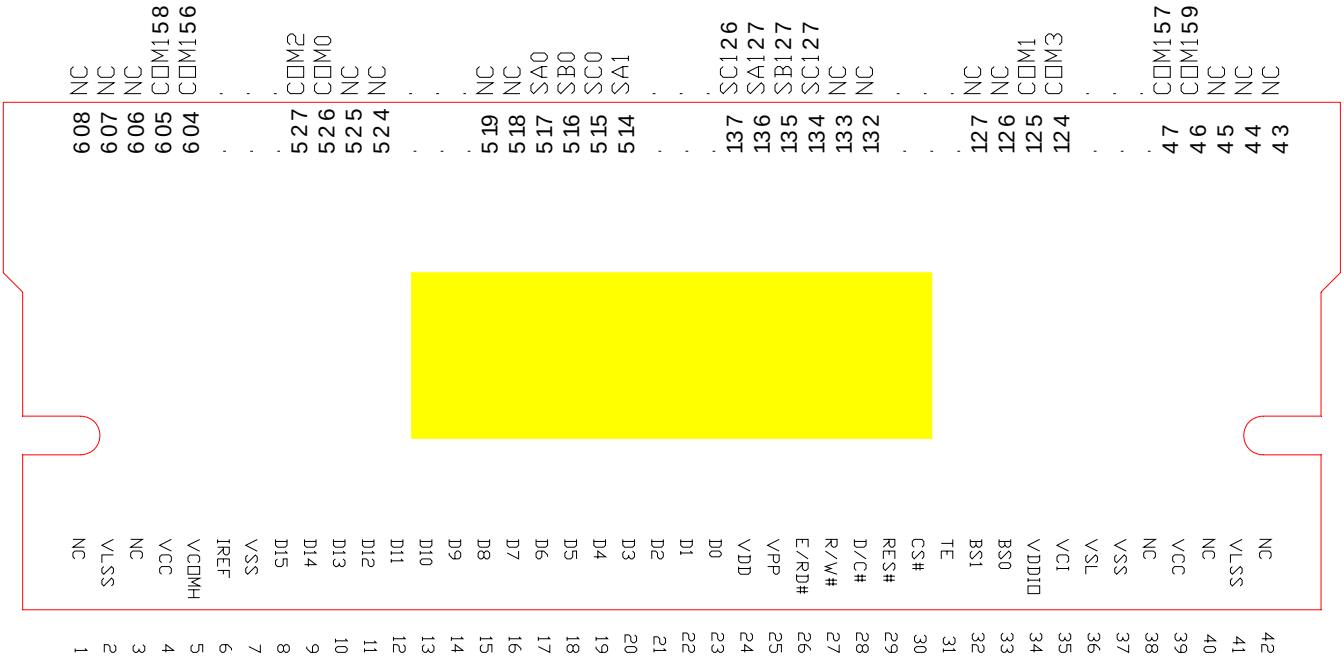


Table 6-3: SSD1355U6R1 Pin Assignment Table

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	NC	81	COM89	161	SC118	241	SA92
2	VLSS	82	COM87	162	SB118	242	SC91
3	NC	83	COM85	163	SA118	243	SB91
4	VCC	84	COM83	164	SC117	244	SA91
5	VCOMH	85	COM81	165	SB117	245	SC90
6	IREF	86	COM79	166	SA117	246	SB90
7	VSS	87	COM77	167	SC116	247	SA90
8	D15	88	COM75	168	SB116	248	SC89
9	D14	89	COM73	169	SA116	249	SB89
10	D13	90	COM71	170	SC115	250	SA89
11	D12	91	COM69	171	SB115	251	SC88
12	D11	92	COM67	172	SA115	252	SB88
13	D10	93	COM65	173	SC114	253	SA88
14	D9	94	COM63	174	SB114	254	SC87
15	D8	95	COM61	175	SA114	255	SB87
16	D7	96	COM59	176	SC113	256	SA87
17	D6	97	COM57	177	SB113	257	SC86
18	D5	98	COM55	178	SA113	258	SB86
19	D4	99	COM53	179	SC112	259	SA86
20	D3	100	COM51	180	SB112	260	SC85
21	D2	101	COM49	181	SA112	261	SB85
22	D1	102	COM47	182	SC111	262	SA85
23	D0	103	COM45	183	SB111	263	SC84
24	VDD	104	COM43	184	SA111	264	SB84
25	VPP	105	COM41	185	SC110	265	SA84
26	E/RD#	106	COM39	186	SB110	266	SC83
27	R/W#	107	COM37	187	SA110	267	SB83
28	D/C#	108	COM35	188	SC109	268	SA83
29	RES#	109	COM33	189	SB109	269	SC82
30	CS#	110	COM31	190	SA109	270	SB82
31	TE	111	COM29	191	SC108	271	SA82
32	BS1	112	COM27	192	SB108	272	SC81
33	BS0	113	COM25	193	SA108	273	SB81
34	VDDIO	114	COM23	194	SC107	274	SA81
35	VCI	115	COM21	195	SB107	275	SC80
36	VSL	116	COM19	196	SA107	276	SB80
37	VSS	117	COM17	197	SC106	277	SA80
38	NC	118	COM15	198	SB106	278	SC79
39	VCC	119	COM13	199	SA106	279	SB79
40	NC	120	COM11	200	SC105	280	SA79
41	VLSS	121	COM9	201	SB105	281	SC78
42	NC	122	COM7	202	SA105	282	SB78
43	NC	123	COM5	203	SC104	283	SA78
44	NC	124	COM3	204	SB104	284	SC77
45	NC	125	COM1	205	SA104	285	SB77
46	COM159	126	NC	206	SC103	286	SA77
47	COM157	127	NC	207	SB103	287	SC76
48	COM155	128	NC	208	SA103	288	SB76
49	COM153	129	NC	209	SC102	289	SA76
50	COM151	130	NC	210	SB102	290	SC75
51	COM149	131	NC	211	SA102	291	SB75
52	COM147	132	NC	212	SC101	292	SA75
53	COM145	133	NC	213	SB101	293	SC74
54	COM143	134	SC127	214	SA101	294	SB74
55	COM141	135	SB127	215	SC100	295	SA74
56	COM139	136	SA127	216	SB100	296	SC73
57	COM137	137	SC126	217	SA100	297	SB73
58	COM135	138	SB126	218	SC99	298	SA73
59	COM133	139	SA126	219	SB99	299	SC72
60	COM131	140	SC125	220	SA99	300	SB72
61	COM129	141	SB125	221	SC98	301	SA72
62	COM127	142	SA125	222	SB98	302	SC71
63	COM125	143	SC124	223	SA98	303	SB71
64	COM123	144	SB124	224	SC97	304	SA71
65	COM121	145	SA124	225	SB97	305	SC70
66	COM119	146	SC123	226	SA97	306	SB70
67	COM117	147	SB123	227	SC96	307	SA70
68	COM115	148	SA123	228	SB96	308	SC69
69	COM113	149	SC122	229	SA96	309	SB69
70	COM111	150	SB122	230	SC95	310	SA69
71	COM109	151	SA122	231	SB95	311	SC68
72	COM107	152	SC121	232	SA95	312	SB68
73	COM105	153	SB121	233	SC94	313	SA68
74	COM103	154	SA121	234	SB94	314	SC67
75	COM101	155	SC120	235	SA94	315	SB67
76	COM99	156	SB120	236	SC93	316	SA67
77	COM97	157	SA120	237	SB93	317	SC66
78	COM95	158	SC119	238	SA93	318	SB66
79	COM93	159	SB119	239	SC92	319	SA66
80	COM91	160	SA119	240	SB92	320	SC65

Pin No.	Pin Name
321	SB65
322	SA65
323	SC64
324	SB64
325	SA64
326	SC63
327	SB63
328	SA63
329	SC62
330	SB62
331	SA62
332	SC61
333	SB61
334	SA61
335	SC60
336	SB60
337	SA60
338	SC59
339	SB59
340	SA59
341	SC58
342	SB58
343	SA58
344	SC57
345	SB57
346	SA57
347	SC56
348	SB56
349	SA56
350	SC55
351	SB55
352	SA55
353	SC54
354	SB54
355	SA54
356	SC53
357	SB53
358	SA53
359	SC52
360	SB52
361	SA52
362	SC51
363	SB51
364	SA51
365	SC50
366	SB50
367	SA50
368	SC49
369	SB49
370	SA49
371	SC48
372	SB48
373	SA48
374	SC47
375	SB47
376	SA47
377	SC46
378	SB46
379	SA46
380	SC45
381	SB45
382	SA45
383	SC44
384	SB44
385	SA44
386	SC43
387	SB43
388	SA43
389	SC42
390	SB42
391	SA42
392	SC41
393	SB41
394	SA41
395	SC40
396	SB40
397	SA40
398	SC39
399	SB39
400	SA39

Pin No.	Pin Name
401	SC38
402	SB38
403	SA38
404	SC37
405	SB37
406	SA37
407	SC36
408	SB36
409	SA36
410	SC35
411	SB35
412	SA35
413	SC34
414	SB34
415	SA34
416	SC33
417	SB33
418	SA33
419	SC32
420	SB32
421	SA32
422	SC31
423	SB31
424	SA31
425	SC30
426	SB30
427	SA30
428	SC29
429	SB29
430	SA29
431	SC28
432	SB28
433	SA28
434	SC27
435	SB27
436	SA27
437	SC26
438	SB26
439	SA26
440	SC25
441	SB25
442	SA25
443	SC24
444	SB24
445	SA24
446	SC23
447	SB23
448	SA23
449	SC22
450	SB22
451	SA22
452	SC21
453	SB21
454	SA21
455	SC20
456	SB20
457	SA20
458	SC19
459	SB19
460	SA19
461	SC18
462	SB18
463	SA18
464	SC17
465	SB17
466	SA17
467	SC16
468	SB16
469	SA16
470	SC15
471	SB15
472	SA15
473	SC14
474	SB14
475	SA14
476	SC13
477	SB13
478	SA13
479	SC12
480	SB12

Pin No.	Pin Name
481	SA12
482	SC11
483	SB11
484	SA11
485	SC10
486	SB10
487	SA10
488	SC9
489	SB9
490	SA9
491	SC8
492	SB8
493	SA8
494	SC7
495	SB7
496	SA7
497	SC6
498	SB6
499	SA6
500	SC5
501	SB5
502	SA5
503	SC4
504	SB4
505	SA4
506	SC3
507	SB3
508	SA3
509	SC2
510	SB2
511	SA2
512	SC1
513	SB1
514	SA1
515	SC0
516	SB0
517	SA0
518	NC
519	NC
520	NC
521	NC
522	NC
523	NC
524	NC
525	NC
526	COM0
527	COM2
528	COM4
529	COM6
530	COM8
531	COM10
532	COM12
533	COM14
534	COM16
535	COM18
536	COM20
537	COM22
538	COM24
539	COM26
540	COM28
541	COM30
542	COM32
543	COM34
544	COM36
545	COM38
546	COM40
547	COM42
548	COM44
549	COM46
550	COM48
551	COM50
552	COM52
553	COM54
554	COM56
555	COM58
556	COM60
557	COM62
558	COM64
559	COM66
560	COM68

Pin No.	Pin Name
561	COM70
562	COM72
563	COM74
564	COM76
565	COM78
566	COM80
567	COM82
568	COM84
569	COM86
570	COM88
571	COM90
572	COM92
573	COM94
574	COM96
575	COM98
576	COM100
577	COM102
578	COM104
579	COM106
580	COM108
581	COM110
582	COM112
583	COM114
584	COM116
585	COM118
586	COM120
587	COM122
588	COM124
589	COM126
590	COM128
591	COM130
592	COM132
593	COM134
594	COM136
595	COM138
596	COM140
597	COM142
598	COM144
599	COM146
600	COM148
601	COM150
602	COM152
603	COM154
604	COM156
605	COM158
606	NC
607	NC
608	NC

7 PIN DESCRIPTIONS

Key:

I = Input	NC = Not Connected
O =Output	Pull LOW= connect to Ground
I/O = Bi-directional (input/output)	Pull HIGH= connect to V_{DDIO}
P = Power pin	

Table 7-1 : SSD1355 Pin Description

Pin Name	Pin Type	Description
V_{DD}	P	Power supply pin for core logic operation. V_{DD} can be supplied externally (within the range of 2.4V to 2.6V) or regulated internally from V_{CI}. A capacitor should be connected between V_{DD} and V_{SS} under all circumstances. Refer to Section 8.11 for details.
V_{DDIO}	P	Power supply for interface logic level. It should match with the MCU interface voltage level and must be connected to external source.
V_{CI}	P	Low voltage power supply V_{CI} must always be equal to or higher than V_{DD} and V_{DDIO}. Refer to Section 8.11 for details.
V_{CC}	P	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. It is supplied by external high voltage source.
V_{PP}	P	Power supply for programming OTP. In OTP programming, this pin is powered up to 7.5V. Refer to Section 9.3.32 OTP Write (B1h) for details. In operation mode (without programming OTP), this pin must be connected to V_{DD}.
V_{SS}	P	Ground pin
V_{LSS}	P	Analog system ground pin
V_{COMH}	P	COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS}.
BGGND	P	It should be connected to Ground.
GPIO0	I/O	Refer to section 9.3.47 GPIO (D7h).
GPIO1	I/O	Refer to section 9.3.47 GPIO (D7h).
VSL	P	This is segment voltage reference pin. When external VSL is not used, this pin should be left open. When external VSL is used, connect with resistor and diode to ground. (details depend on application)

<table>
<tr><th>Pin Name</th><th>Pin Type</th><th>Description</th></tr>
<tr><td>BS[1:0]</td><td>I</td><td>MCU bus interface selection pins. Select appropriate logic setting as described in the following table. BS3 and BS2 are command programmable (by command 36h). [reset = 00]. BS1 and BS0 are pin select.

Table 7-2 : Bus Interface selection
<table><tr><td>BS[3:0]</td><td>Interface</td></tr><tr><td>0000</td><td>4 line SPI</td></tr><tr><td>0001</td><td>3 line SPI</td></tr><tr><td>0011</td><td>8-bit 6800 parallel</td></tr><tr><td>0010</td><td>8-bit 8080 parallel</td></tr><tr><td>0111</td><td>16-bit 6800 parallel</td></tr><tr><td>0110</td><td>16-bit 8080 parallel</td></tr><tr><td>1111</td><td>18-bit 6800 parallel</td></tr><tr><td>1110</td><td>18-bit 8080 parallel</td></tr></table>Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DDIO}</td></tr>
<tr><td>I_{REF}</td><td>I</td><td>This pin is the segment output current reference pin.

I_{REF} can be supplied externally or regulated internally.

When external I_{REF} is selected, a resistor should be connected between this pin and V_{SS}. When internal I_{REF} is selected, this pin should be floated.</td></tr>
<tr><td>CL</td><td>I</td><td>External clock input pin.

When internal clock is enable (i.e. pull HIGH in CLS pin), this pin is not used and should be connected to Ground.
When internal clock is disable (i.e. pull LOW is CLS pin), this pin is the external clock source input pin.</td></tr>
<tr><td>CLS</td><td>I</td><td>Internal clock selection pin.

When this pin is pulled HIGH, internal oscillator is enabled (normal operation).
When this pin is pulled LOW, an external clock signal should be connected to CL.</td></tr>
<tr><td>CS#</td><td>I</td><td>This pin is the chip select input connecting to the MCU.

The chip is enabled for MCU communication only when CS# is pulled LOW.</td></tr>
<tr><td>RES#</td><td>I</td><td>This pin is reset signal input.

When the pin is pulled LOW, initialization of the chip is executed.
Keep this pin pull HIGH during normal operation.</td></tr>
<tr><td>D/C#</td><td>I</td><td>This pin is Data/Command control pin connecting to the MCU.

When the pin is pulled HIGH, the data at D[17:0] will be interpreted as data.
When the pin is pulled LOW, the data at D[17:0] will be interpreted as command.</td></tr>
<tr><td>R/W# (WR#)</td><td>I</td><td>This pin is read / write control input pin connecting to the MCU interface.

When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW.

When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected.</td></tr>
</table>

Pin Name	Pin Type	Description
		When serial interface is selected, this pin R/W (WR#) will be SCLK.
E (RD#)	I	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to V_{SS}.
D[17:0]	I/O	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. (Except for D1 pin in SPI mode)
TE	O	Tearing Effect. To synchronize the MPU to the frame display writing. Do not connect if not used.
SA[127:0] SB[127:0] SC[127:0]	O	These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF. The 384 segment pins are divided into 3 groups, SA, SB and SC. Each group can have different color settings for color A, B and C.
COM[159:0]	I/O	These pins provide the Common switch signals to the OLED panel.

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface

SSD1355 MCU interface consist of 18 data pin and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[1:0] pins and software command on BS[3:0].(refer to Table 7-2 for BS[3:0] setting)

Table 8-1 : MCU interface assignment under different bus interface mode

Pin Name / Bus Interface	Data / Command Interface																Control Signal				
	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	E	R/W#	CS#	D/C#	RES#
8b / 8080	Tie Low										D[7:0]								RD#	WR#	CS#	D/C#	RES#
8b / 6800	Tie Low										D[7:0]								E	R/W#	CS#	D/C#	RES#
16b / 8080	Tie Low	D[15:0]																	RD#	WR#	CS#	D/C#	RES#
16b / 6800	Tie Low	D[15:0]																	E	R/W#	CS#	D/C#	RES#
18b / 8080	D[17:0]																		RD#	WR#	CS#	D/C#	RES#
18b / 6800	D[17:0]																		E	R/W#	CS#	D/C#	RES#
3-wrie SPI	Tie Low																NC	SDIN	Tie Low	SCLK	CS#	Tie Low	RES#
4-wire SPI	Tie Low																NC	SDIN	Tie Low	SCLK	CS#	D/C#	RES#

Table 8-2 : Data bus selection modes

	6800 – series Parallel Interface	**8080 – series Parallel Interface**	**3-wire Serial Interface or 4-wire Serial Interface**
Data Read	18-/16-/8-bits	18-/16-/8-bits	No
Data Write	18-/16-/8-bits	18-/16-/8-bits	8-bits
Command Read	Yes. Refer to section 9	Yes. Refer to section 9	No
Command Write	Yes	Yes	Yes

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 18 bi-directional data pins (D[17:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.
A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

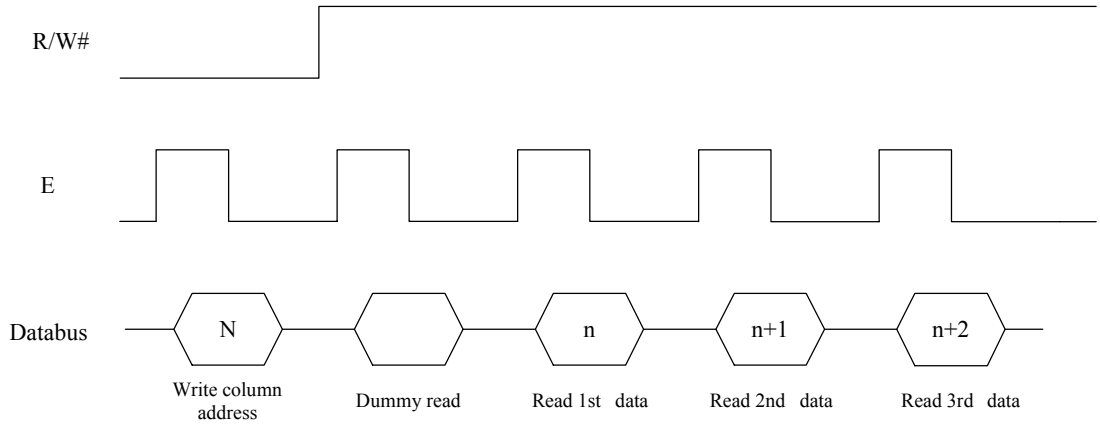
Table 8-3 : Control pins of 6800 interface

Function	**E**	**R/W#**	**CS#**	**D/C#**
Write command	↓	L	L	L
Read status	↓	H	L	L
Write data	↓	L	L	H
Read data	↓	H	L	H

Note
(1) ↓ stands for falling edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 18 bi-directional data pins (D[17:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.
A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.
A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

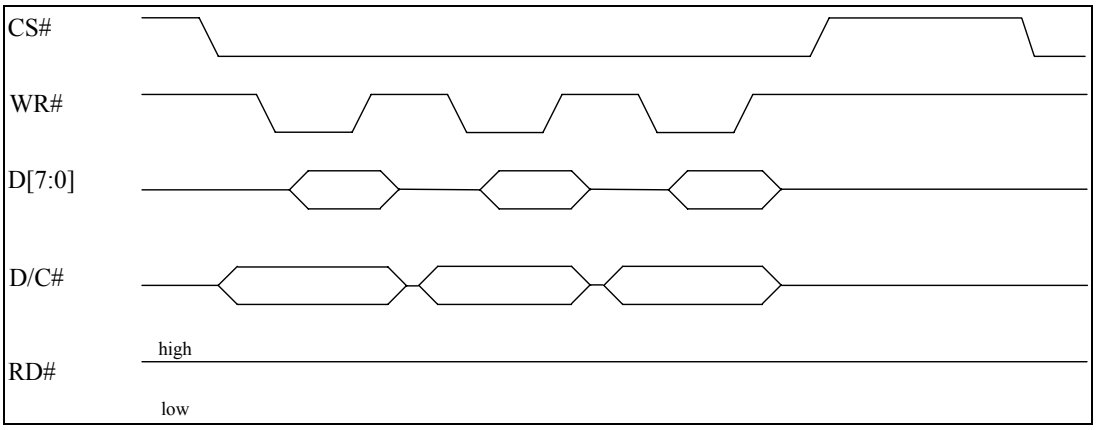


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

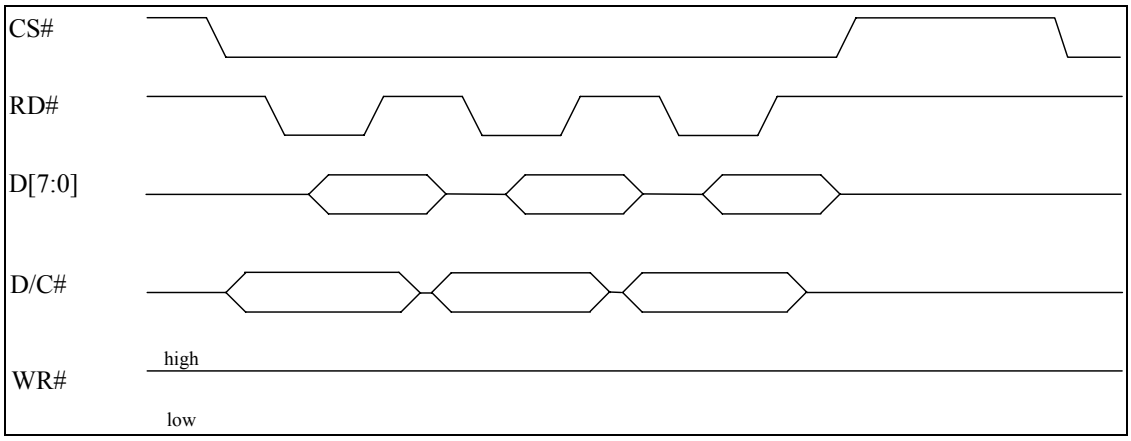


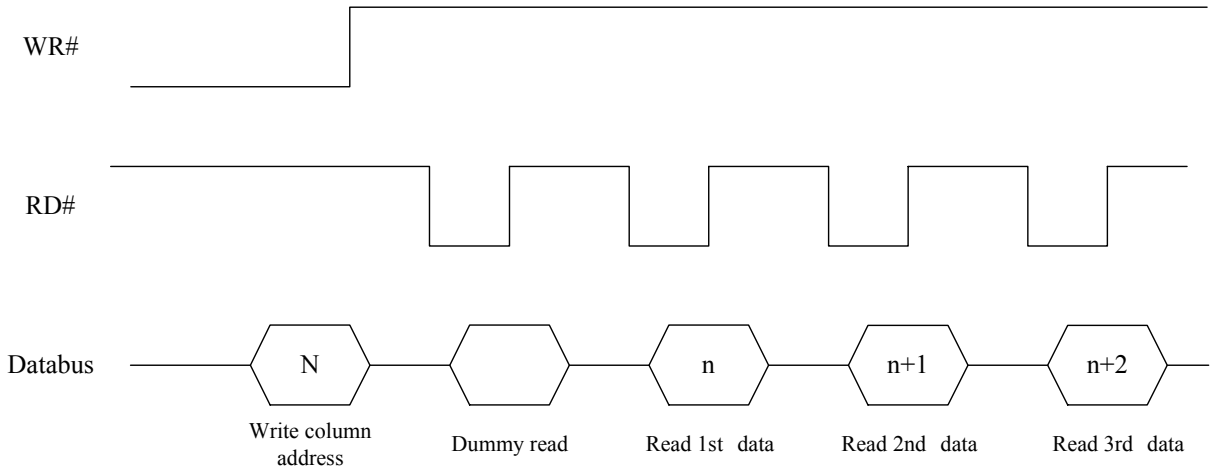
Table 8-4 : Control pins of 8080 interface

Function	RD#	WR#	CS#	D/C#
Write command	H	↑	L	L
Read status	↑	H	L	L
Write data	H	↑	L	H
Read data	↑	H	L	H

Note
(1) ↑ stands for rising edge of signal
(2) H stands for HIGH in signal
(3) L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface (4-wire SPI)

The 4-wire serial interface consists of serial clock: SCLK, serial data: SDIN, D/C#, CS#. In 4-wire SPI mode, R/W# (WR#) acts as SCLK, D0 acts as SDIN. For the unused data pins, D1 should be left open. The pins from D2 to D17and E can be connected to an external ground.

Table 8-5 : Control pins of 4-wire Serial interface

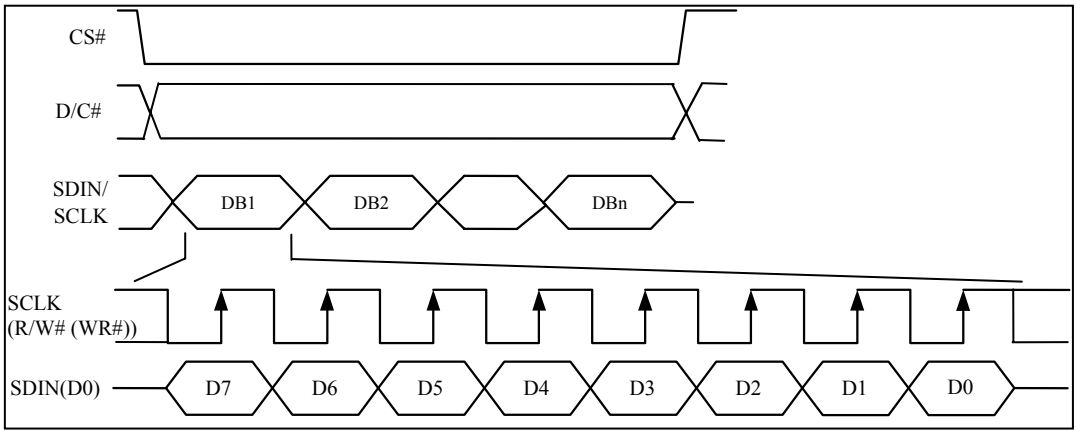
Function	E	CS#	D/C#
Write command	Tie LOW	L	L
Write data	Tie LOW	L	H

Note
(1) H stands for HIGH in signal
(2) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in 4-wire Serial interface mode



8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.
In 3-wire SPI mode, R/W# (WR#) acts as SCLK, D0 acts as SDIN. For the unused data pins, D1 should be left open. The pins from D2 to D17, E and D/C# can be connected to an external ground.

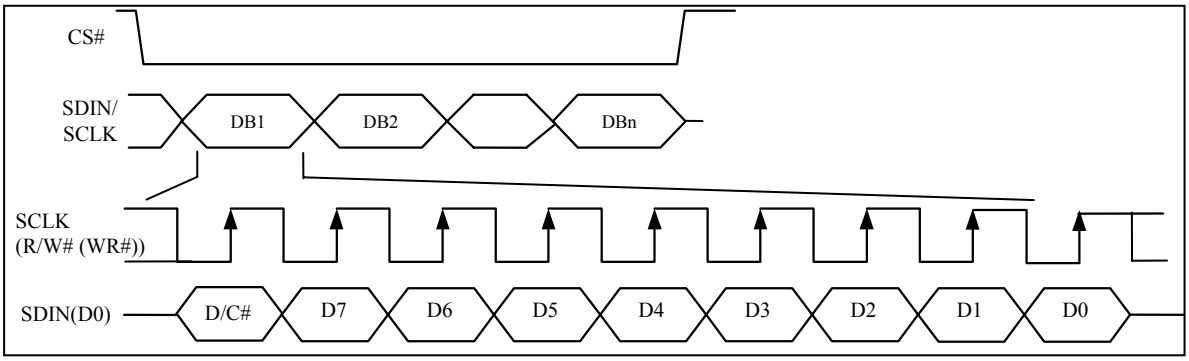
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 8-6 : Control pins of 3-wire Serial interface

Function	E	R/W#	CS#	D/C#
Write command	Tie LOW	SCLK	L	Tie LOW
Write data	Tie LOW	SCLK	L	Tie LOW

Note
(1) L stands for LOW in signal

Figure 8-6 : Write procedure in 3-wire Serial interface mode



8.2 Reset Circuit

When RES# input is pulled LOW, the chip is initialized with the following status:

1. Display is OFF
2. 160 MUX Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Individual contrast control registers of color A, B, and C are set at 80h

8.3 GDDRAM

8.3.1 GDDRAM structure

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 128 x 160 x 18bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Each pixel has 18-bit data. Each sub-pixels for color A, B and C have 6 bits. The arrangement of data pixel in graphic display data RAM is shown in Table 8-7

Table 8-7 : 262k Color Depth Graphic Display Data RAM Structure

Segment	Normal	0			1			2	……	……	126	127		
Address	Remapped	127			126			125	……	……	1	0		
Color		A	B	C	A	B	C	A			C	A	B	C
Data Format / Common Address		A5	B5	C5	A5	B5	C5	A5	……	……	C5	A5	B5	C5
		A4	B4	C4	A4	B4	C4	A4	……	……	C4	A4	B4	C4
		A3	B3	C3	A3	B3	C3	A3	……	……	C3	A3	B3	C3
		A2	B2	C2	A2	B2	C2	A2	……	……	C2	A2	B2	C2
		A1	B1	C1	A1	B1	C1	A1	……	……	C1	A1	B1	C1
		A0	B0	C0	A0	B0	C0	A0	……	……	C0	A0	B0	C0
Normal	Remapped													
0	159	6	6	6	6	6	6	6	……	……	6	6	6	6
1	158	6	6	6	6	6	6	6	……	……	6	6	6	6
2	157	6	6	6	6	6	6	6	……	……	6	6	6	6
3	156	6	6	6	6	6	6	6	……	……	6	6	6	6
4	155	6	6	6	6	6	6	6	……	……	6	6	6	6
5	154	6	6	6	6	6	6	6	……	……	6	6	6	6
6	153	6	6	no of bits in this cell			6	6	……	……	6	6	6	6
7	152								……	……	6	6	6	6
:	:	:	:	:	:	:	:	:	……	……	:	:	:	:
:	:	:	:	:	:	:	:	:	……	……	:	:	:	:
:	:	:	:	:	:	:	:	:	……	……	:	:	:	:
155	4	6	6	6	6	6	6	6	……	……	6	6	6	6
156	3	6	6	6	6	6	6	6	……	……	6	6	6	6
157	2	6	6	6	6	6	6	6	……	……	6	6	6	6
158	1	6	6	6	6	6	6	6	……	……	6	6	6	6
159	0	6	6	6	6	6	6	6	……	……	6	6	6	6

Common output
COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
:
:
:
:
COM156
COM157
COM158
COM159

SEG output	SA0	SB0	SC0	SA1	SB1	SC1	SA2	……	……	SC126	SA127	SB127	SC127

8.3.2 Data bus to RAM mapping under different input mode

Table 8-8 : Write Data bus usage under different bus width and color depth mode

Write Data			Data bus D[17:0]																	
Bus width	Color Depth	Input order	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8 bits / SPI	65k	1st	X	X	X	X	X	X	X	X	X	X	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3
		2nd	X	X	X	X	X	X	X	X	X	X	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0
8 bits / SPI	262k	1st	X	X	X	X	X	X	X	X	X	X	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	X	X
		2nd	X	X	X	X	X	X	X	X	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	X	X
		3rd	X	X	X	X	X	X	X	X	X	X	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	X	X
16 bits	65k		X	X	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_4	A_3	A_2	A_1	A_0
16 bits	262k	1st	X	X	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	X	X
		2nd	X	X	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	X	X	$C2_5$	$C2_4$	$C2_3$	$C2_2$	$C2_1$	$C2_0$	X	X
		3rd	X	X	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	X	X	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$	X	X
18 bits	262k		C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0

Table 8-9 : Read Data bus usage under different bus width and color depth mode

Read Data		Data bus D[17:0]																	
Bus width	Output order	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8 bits	1st	X	X	X	X	X	X	X	X	X	X	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	X	X
	2nd	X	X	X	X	X	X	X	X	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	X	X
	3rd	X	X	X	X	X	X	X	X	X	X	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	X	X
16 bits	1st	X	X	$C1_5$	$C1_4$	$C1_3$	$C1_2$	$C1_1$	$C1_0$	X	X	$B1_5$	$B1_4$	$B1_3$	$B1_2$	$B1_1$	$B1_0$	X	X
	2nd	X	X	$A1_5$	$A1_4$	$A1_3$	$A1_2$	$A1_1$	$A1_0$	X	X	$C2_5$	$C2_4$	$C2_3$	$C2_2$	$C2_1$	$C2_0$	X	X
	3rd	X	X	$B2_5$	$B2_4$	$B2_3$	$B2_2$	$B2_1$	$B2_0$	X	X	$A2_5$	$A2_4$	$A2_3$	$A2_2$	$A2_1$	$A2_0$	X	X
18 bits		C_5	C_4	C_3	C_2	C_1	C_0	B_5	B_4	B_3	B_2	B_1	B_0	A_5	A_4	A_3	A_2	A_1	A_0

Note

(1) The Read Data bus usage is independent of color depth.

8.4 Command Decoder

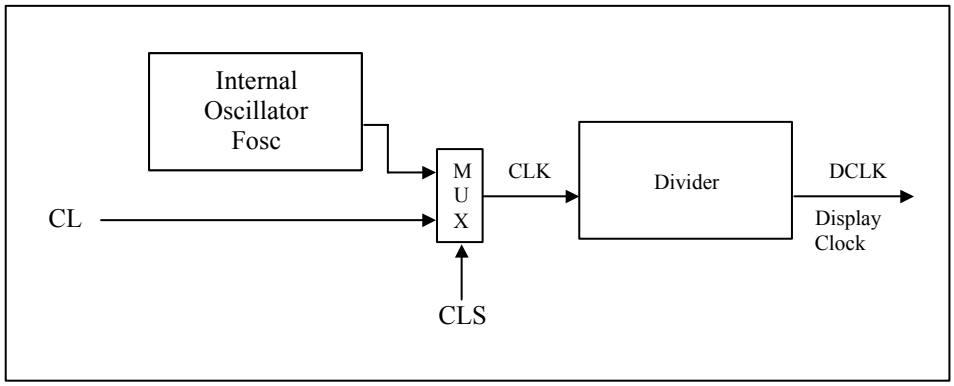
This module determines whether the input should be interpreted as data or command based upon the input of the D/C# pin.

If D/C# pin is HIGH, data is written to Graphic Display Data RAM (GDDRAM). If it is LOW, the inputs at D0-D17 are interpreted as a Command and it will be decoded and be written to the corresponding command register.

8.5 Oscillator & Timing Generator

8.5.1 Oscillator

Figure 8-7 : Oscillator Circuit



This module is an On-Chip low power RC oscillator circuitry (Figure 8-7). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin by CLS pin. If CLS pin is HIGH, internal oscillator is selected. If CLS pin is LOW, external clock from CL pin will be used for CLK. The frequency of internal oscillator F_{OSC} can be programmed by command D2h.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor "D" can be programmed from 1 to 16 by command D2h.

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula:

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command D2h A[3:0]. The divide ratio has the range from 1 to 1024 .
- K is the number of display clocks per row. The value is derived by
  K = Phase 1 period +Phase 2 period + 75
  = 9 +7 +75 =91 (reset)
- Number of multiplex ratio is set by command CAh. The reset value is 159 (i.e. 160MUX).
- F_{osc} is the oscillator frequency. It can be changed by command D2h A[7:4]. The higher the register setting results in higher frequency.

If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption on the whole system.

8.6 SEG/COM Driving block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current for segment current drivers I_{SEG}. The relationship between reference current and segment current of a color is:

  I_{SEG} = Contrast / 256 * I_{REF} * scale factor

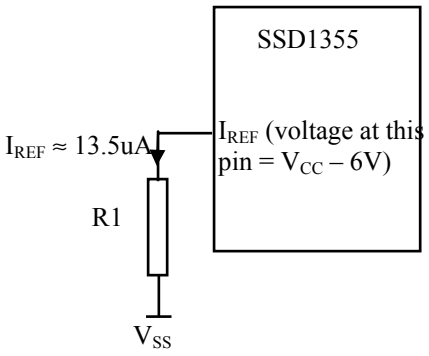
  in which
  the contrast is set by Set Contrast command (BAh, BBh, BCh); and
  the scale factor (1 ~ 16) is set by Master Current Control command (51h).

I_{REF} can be supplied externally or internally. Selection is set by Function Selection command (B3h).

When the command B3h, bit A[6] is set to 1b, the internal I_{REF} regulator is enabled. The typical regulated I_{REF} is about 13.5uA. When the command B3h, bit A[0] is set to 0b, external I_{REF} is selected. A resistor should be connected between I_{REF} pin and Vss pin.

For example, in case external I_{REF} is selected and target I_{REF} is about 13.5uA, the appropriate I_{REF} resistor between I_{REF} pin to V_{SS} pin should has a value as shown in Figure 8-8.

Figure 8-8 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is V_{CC} – 6V, the value of resistor R1 can be found as below:

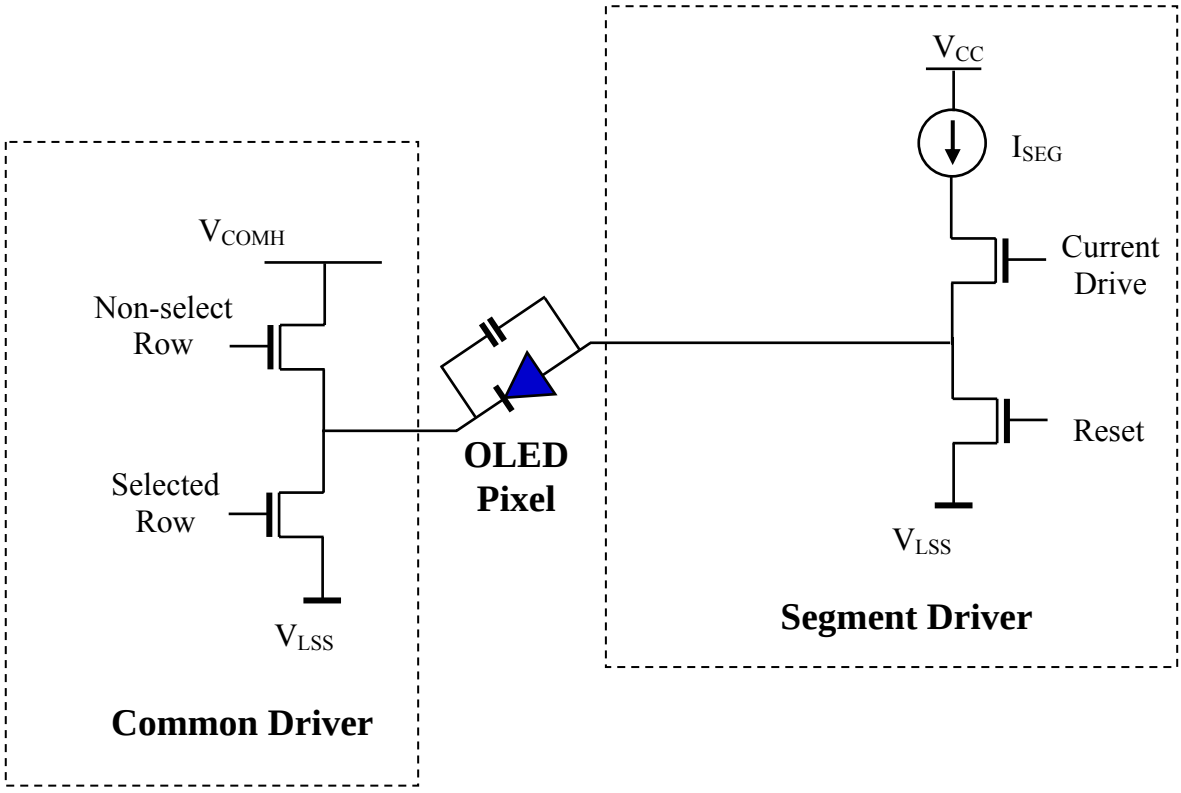
For I_{REF} = 13.5uA, V_{CC} =18V:

R1 = (Voltage at I_{REF} – V_{SS}) / I_{REF}
≈ (18 – 6) / 13.5uA
≈ 880KΩ

8.7 SEG / COM Driver

Segment drivers consist of 384 (128 x 3 colors) current sources to drive OLED panel. The driving current can be adjusted from 0 to 200uA with 256 steps by contrast setting command (BAh, BBh, BCh). Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

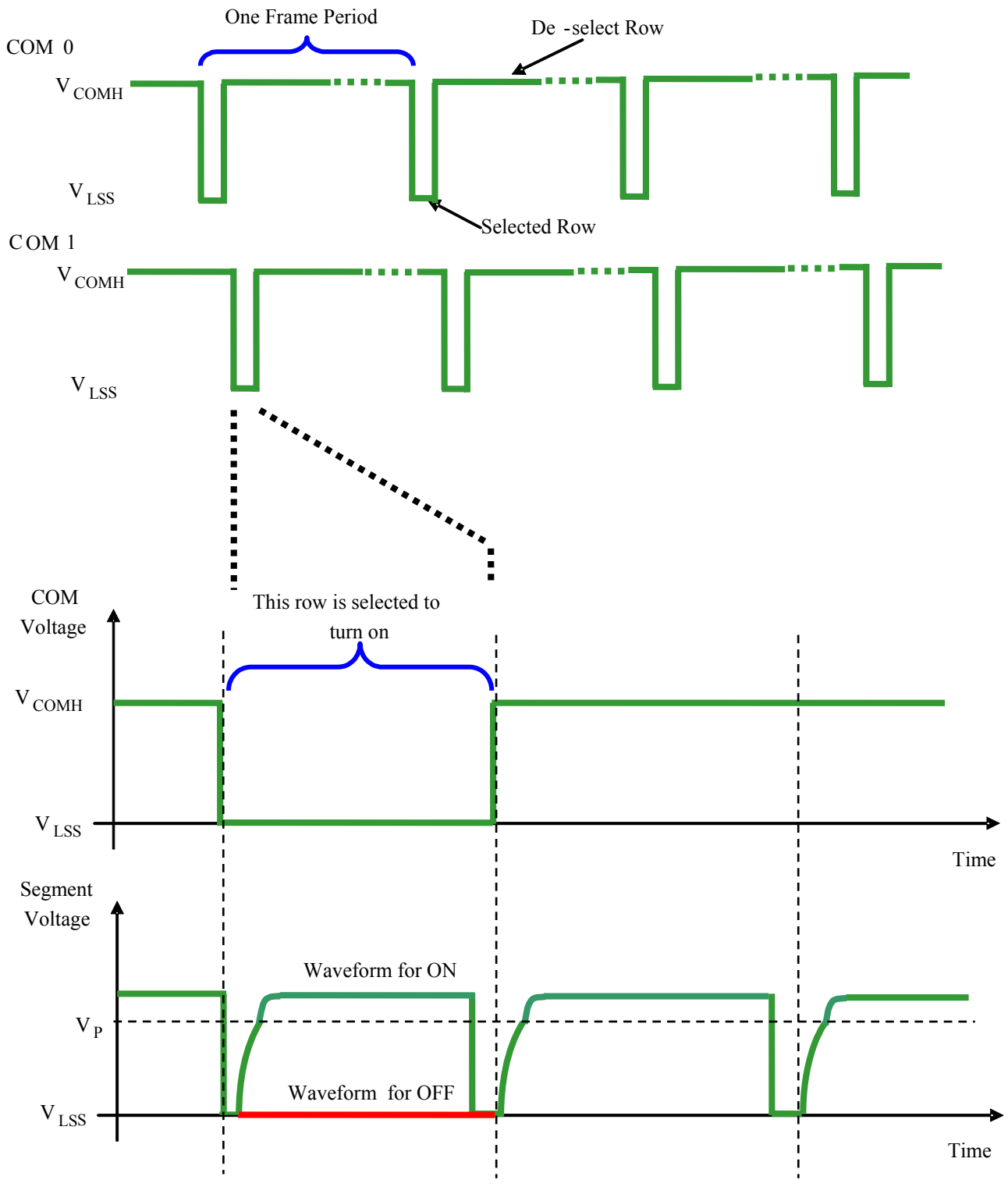
Figure 8-9 : Segment and Common Driver Block Diagram



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 8-10.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is disabled and the Reset switch is enabled. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 8-10 : Segment and Common Driver Signal Waveform



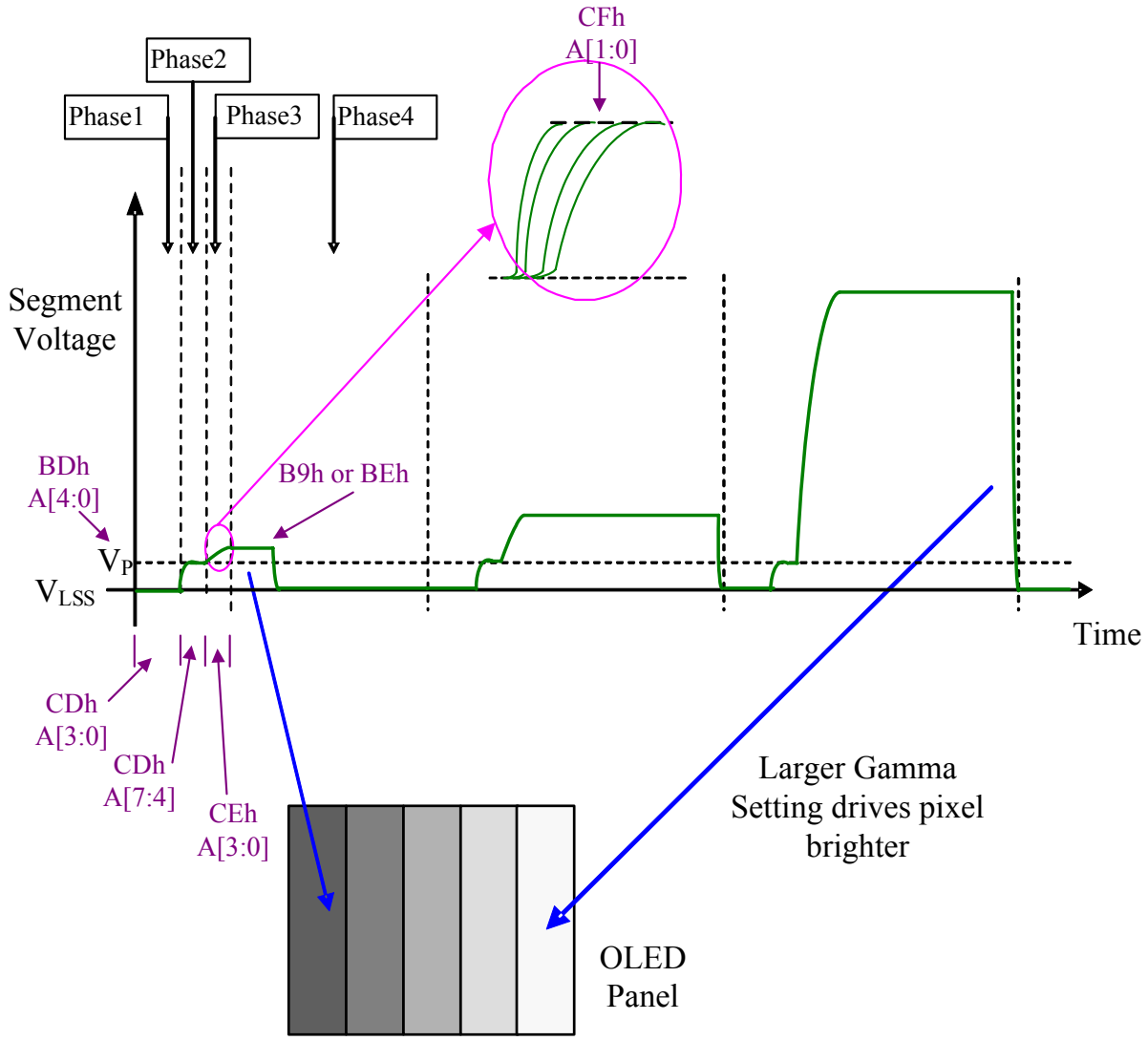
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command CDh A[3:0]. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS}. The amplitude of V_P can be programmed by the command BDh. The period of phase 2 can be programmed by command CDh A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by command CEh.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PAM+PWM (Pulse Area Modulation + Pulse Width Modulation) method to control the gray scale of each pixel individually. The gray scale can be programmed into different Gamma settings by command B9h/BEh. The bigger gamma setting in the current drive stage results in brighter pixels and vice versa (Details refer to Section 8.8). This is shown in the following figure.

Figure 8-11: Gray Scale Control in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle runs continuously to refresh image display on OLED panel.

8.8 Gray Scale Decoder

The gray scale effect is generated by controlling the segment current in current drive phase. The segment current is controlled by the Gamma Settings (Setting 0~ Setting 127). The larger the setting, the brighter the pixel will be. The Gray Scale Table stores the corresponding Gamma Setting of the 64 gray scale levels (GS0~GS63) through the software commands BEh or B9h. Three programmable Gray Scale Tables (Gamma Look Up table) support the three colors A, B and C.

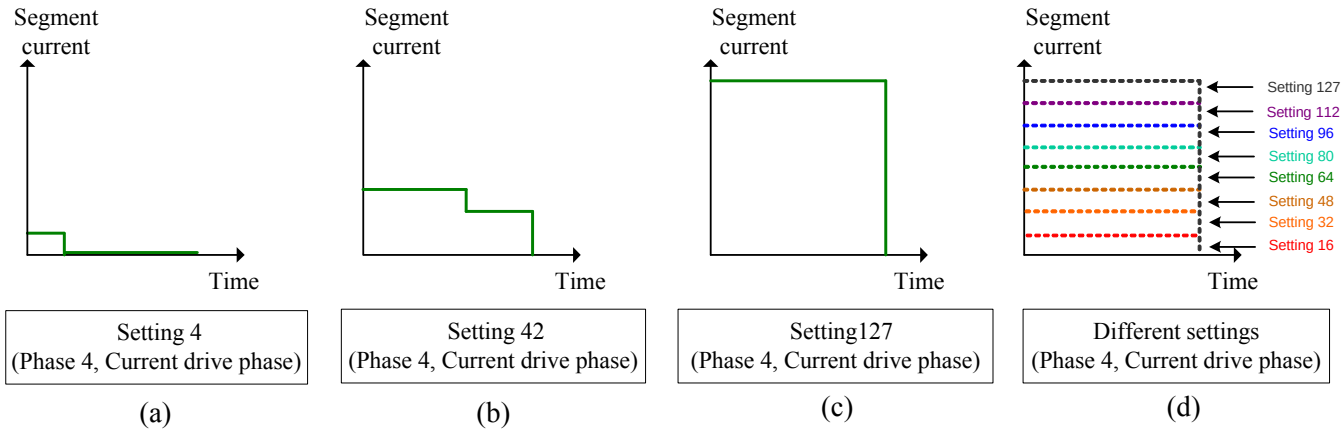
As shown in Figure 8-12, color A, B, C sub-pixel RAM data has 6 bits, represent the 64 gray scale level from GS0 to GS63.

Figure 8-12 : Relation between GDDRAM content and Gray Scale table entry for three colors in 262K color mode (under command B9h Linear Gamma Look Up Table)

Color A, B or C GDDRAM data (6 bits)	Gray Scale Table	Default Gamma Setting (Command B9h Linear Gamma Look Up Table)
000000	GS0	Setting 0
000001	GS1	Setting 2
000010	GS2	Setting 4
000011	GS3	Setting 6
000100	GS4	Setting 8
:	:	:
011111	GS31	Setting 62
100000	GS32	Setting 65
100001	GS33	Setting 67
:	:	:
111100	GS60	Setting 121
111101	GS61	Setting 123
111110	GS62	Setting 125
111111	GS63	Setting 127

The Gray Scale Table can be programmed into different Gamma setting by command BEh. For example, if GS1 is programmed into Gamma setting 4, and the color A, B or C of GDDRAM is set as “000001b”, then the current drive phase will be similar to the illustration in Figure 8-13(a).

Figure 8-13 : Illustration of current drive phase (phase 4) under different Gamma Settings.



There are total 128 Gamma Settings (Setting 0 to Setting 127) available for the Gray Scale table. GS0 has no pre-charge and current drive stages so it is in Gamma Setting 0.

When setting the Gray Scale Table (by BEh command) , the rules below must follow:

1) Only odd Gamma Settings (i.e. GS1, GS3, GS5,.....GS63) are entered after command BEh. SSD1355 will automatically calculate the even Gamma Settings (i.e. GS2, GS4, GS6,.....GS62)

2) The gray scale is defined in incremental way, with reference to the length of previous table entry:

Setting of GS1 must > 0
Setting of GS3 must > Setting of GS1 +1
Setting of GS5 must > Setting of GS3 +1
:
Setting of GS63 must > Setting of GS61 +1

It should be notice that, the brightness under the following pairs of Gamma Setting will be the same:

Table 8-10 : Gamma Settings with identical brightness in current drive phase

Setting 15 & Setting 16	Setting 63 & Setting 64	Setting 111 & Setting 112
Setting 31 & Setting 32	Setting 79 & Setting 80	
Setting 47 & Setting 48	Setting 95 & Setting 96	

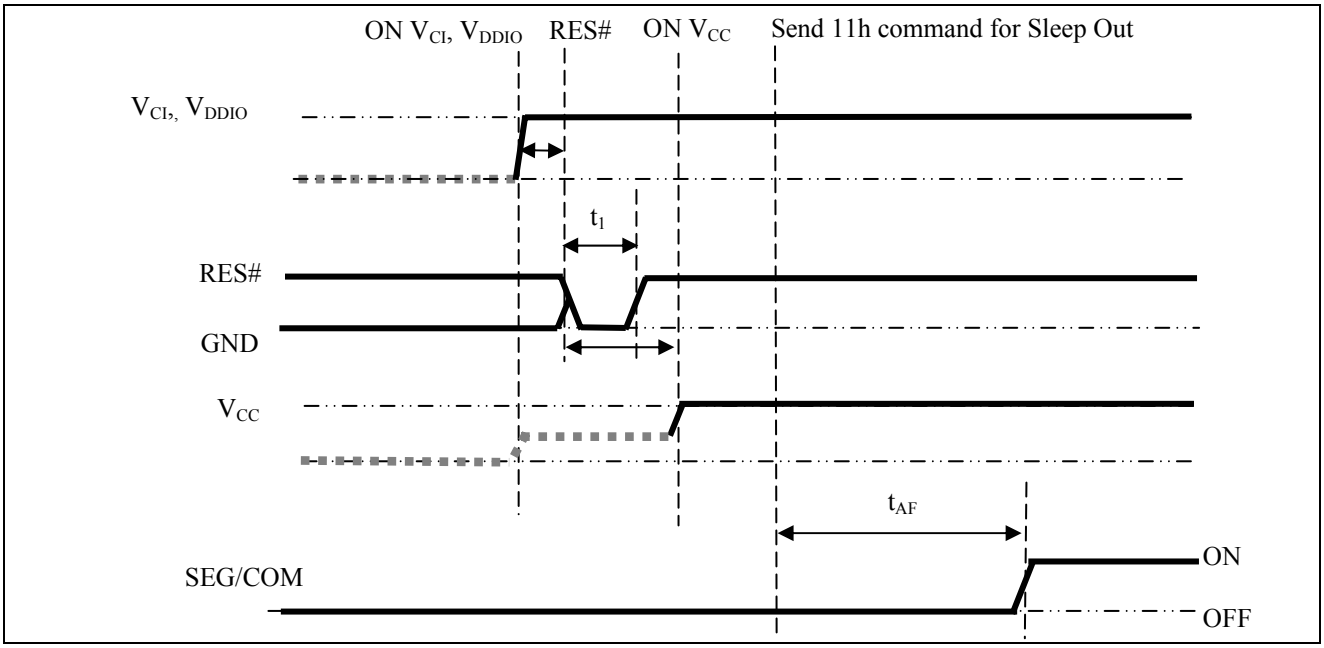
8.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1355 (assume V_{CI} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

Power ON sequence:

1. Power ON $V_{CI,}$ $V_{DDIO.}$
2. After V_{CI}, V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 2us (t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 2us (t_2). Then Power ON $V_{CC.}$ (1)
4. After V_{CC} become stable, send command 11h for Sleep Out. SEG/COM will be ON after 200ms (t_{AF}).

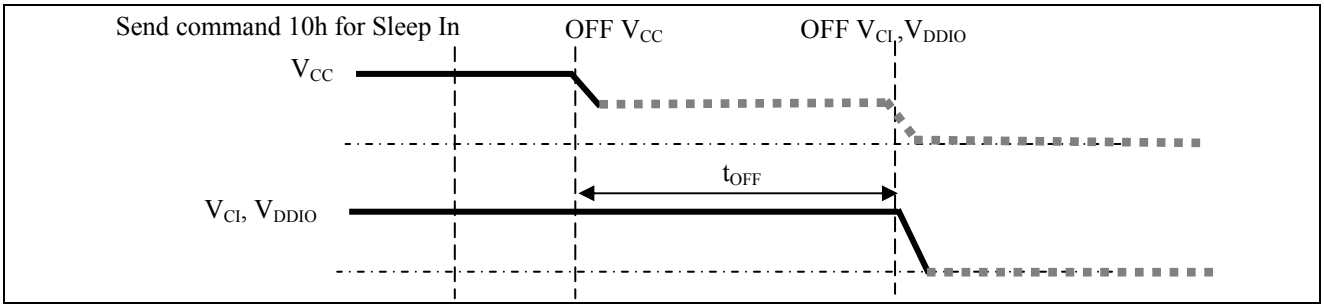
Figure 8-14: The Power ON sequence.



Power OFF sequence:

1. Send command 10h for Sleep In.
2. Power OFF $V_{CC.}$ (1), (2)
3. Wait for t_{OFF}. Power OFF $V_{CI,}$ $V_{DDIO.}$ (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)

Figure 8-15: The Power OFF sequence



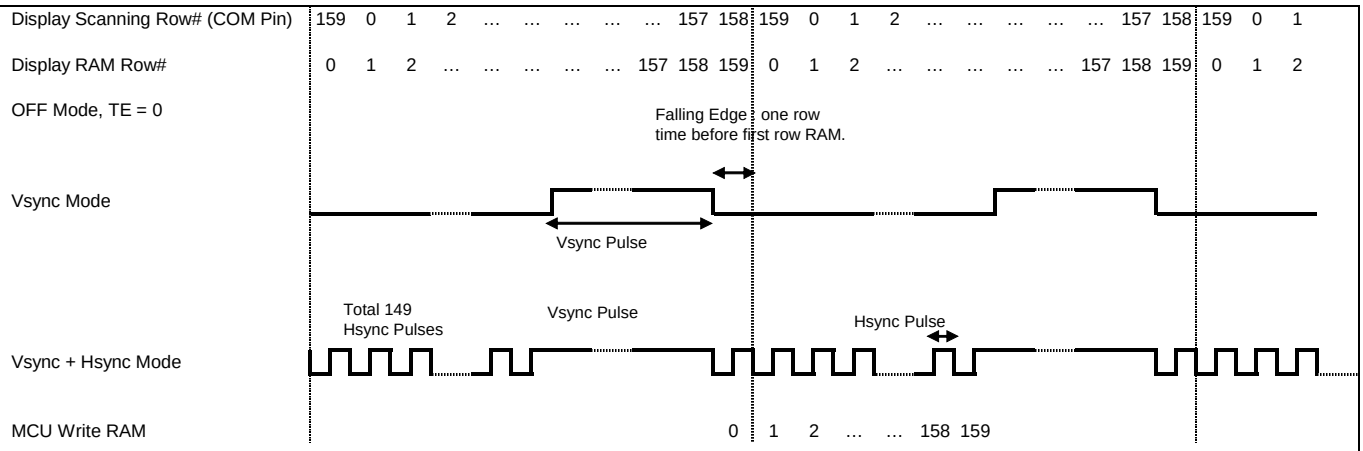
Note:

(1) Since an ESD protection circuit is connected between V_{CI}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{CI} whenever $V_{CI,}$ V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-14 and Figure 8-15.

(2) V_{CC} should be kept float when it is OFF.

8.10 Tearing Effect Timing

TE synchronization signal can be used to prevent tearing effect.



Note:
(1) Assume MCU speed is faster than display speed.
(2) To avoid tearing effect, write the first row (row#=0) of data to RAM right after the falling edge of V-sync pulse.
(3) Hsync pulses are used for much more sophisticated applications.

8.11 V_{DD} Regulator

In SSD1355, the power supply pin for core logic operation: V_{DD}, can be supplied by external source or internally regulated through the V_{DD} regulator.

When the command B3h, bit A[0] is set to 1b, the internal V_{DD} regulator is enabled. V_{CI} should be larger than 2.6V when using the internal V_{DD} regulator. The typical regulated V_{DD} is about 2.5V

When the command B3h, bit A[0] is set to 0b, external V_{DD} should be used. (external V_{DD} range : 2.4V~2.6V)

It should be notice that, no matter V_{DD} is supplied by external source or internally regulated, V_{CI} must always be equal or higher than V_{DD} and V_{DDIO}.

The following figure shows the V_{DD} regulator pin connection scheme:

Figure 8-16 V_{CI} > 2.6V, V_{DD} regulator enable : pin connection scheme

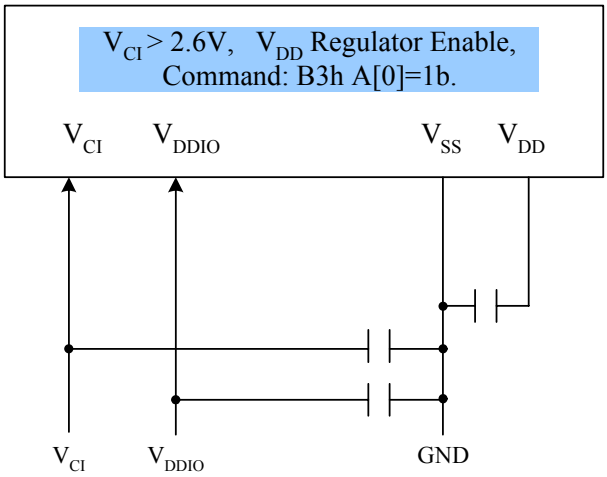
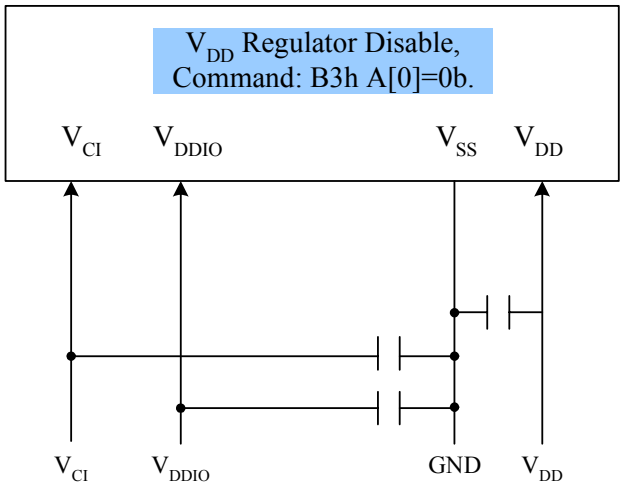


Figure 8-17 V_{DD} regulator disable : pin connection scheme



8.11.1 V_{DD} Regulator in Sleep Mode

Power can be saved by disable the internal V_{DD} regulator during Sleep mode. The following figures show the corresponding command sequence:

Figure 8-18 : Case 1 - Command sequence for just entering/ exiting sleep mode

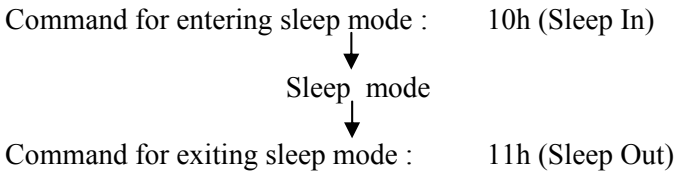
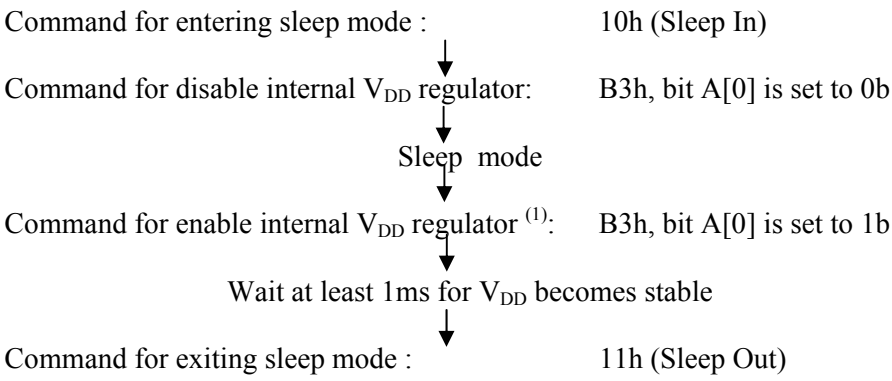


Figure 8-19 : Case 2 - Command sequence for disabling internal V_{DD} regulator during sleep mode



In the above two cases, the RAM content can also be kept during the sleep mode.

Note:
(1) It should be noted that the internal V_{DD} regulator should be enabled before exiting sleep mode (issuing command 11h).
(2) No RAM access through MCU interface when there is no external/ internal V_{DD}.

9 COMMAND

9.1 Basic Command List

Operational Code (Hex)	Function	Bytes of Parameter
00	No Operation (NOP)	0
01	Software Reset (SWRESET)	0
04	Read Display Identification Information (RDDIDIF)	2
0A	Read Display Power Mode (RDDPM)	2
0B	Read Display MADCTL (RDDMADCTL)	2
0C	Read Display Pixel Format (RDDCOLMOD)	2
0D	Read Display Image Mode (RDDIM)	2
0E	Read Display Signal Mode (RDDSM)	2
10	Sleep In (SLPIN)	0
11	Sleep Out (SLPOUT)	0
12	Enable Partial Display (PTLON)	0
13	Normal Display Mode ON (NORON)	0
20	Display Inversion OFF (INVOFF)	0
21	Display Inversion ON (INVON)	0
23	All Pixels ON (ALLPON)	0
28	All Pixels OFF(ALLPOFF)	0
29	Disable All Pixels ON/OFF (DISPON)	0
2A	Set Column Address (CASET)	2
2B	Set Row Address (RASET)	2
2C	Memory Write (RAMWR)	Any length
2E	Memory Read (RAMRD)	Any length
30	Set Partial Display Area (PLTAR)	2
33	Set Vertical Scrolling Areas (VSCRDEF)	3
34	Disable Tearing Effect (TEOFF)	0
35	Enable Tearing Effect (TEON)	1
36	Memory Access Control (MADCTL)	2
37	Vertical Scrolling Start Address(VSCRSADD)	1
3A	Interface Pixel Format (COLMOD)	1
51	Write Luminance (SETLUM)	1
52	Read Luminance (RDLUM)	2
DA	Read Display Identification Information (RDDIDIF)	2

9.2 Supplementary Command List

Operational Code (Hex)	Function	Bytes of Parameter
B1	OTP Write (OTPWR)	3
B2	OTP MCU Read (OTPRD)	3
B3	Function Selection (FUSEL)	1
B9	Linear Gamma Look Up Table (LINGLUT)	0
BA	Set Contrast for Color A,B,C (ISEGABC)	5
BD	Set First Pre-Charge Voltage (VPSET)	1
BE	Gamma Look Up Table (GLUT)	96
C8	Set Display Offset (SETDO)	1
C9	Horizontal Scrolling (HORSCR)	1
CA	Set MUX ratio (SETMUX)	1
CD	Set Phase Length (PHLEN)	1
CE	Set Second Precharge Period (SECPLEN)	1
CF	Set Second Precharge Speed (SSPS)	1
D2	Set Display Clock Divider / Oscillator Frequency (SDCOSCF)	1
D3	Set V_{COMH} (SETVCOMH)	1
D7	GPIO (GPIO)	1
FD	Command Lock (COMLCK)	1

Note

(1) Issue command FDh → B3h to access the above supplementary commands

9.3 Command Description

Note
(1) "xx" stands for "Don't care".

9.3.1 NOP (00h)

00 h	NOP (No Operation)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER											
Description	This is the no operation command. However it can be used to terminate RAM Write or Read as described in RAMWR (2Ch, Memory Write) and RAMRD (2Eh, Memory Read) Commands.											
Command Availability												

Status	Availability
Normal Mode ON, Sleep Out	Yes
Partial Mode ON, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
S/W Reset	N/A
H/W Reset	N/A

9.3.2 Software Reset (01h)

<table>
<tr><th>01 h</th><th colspan="12">SWRESET (Software Reset)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>01</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">When the Software Reset command is written, it causes software reset for the following commands. It resets the commands and parameters to their S/W Reset default values. (See default tables in each command description.)

The display turns OFF after Software Reset command is written.

Software Reset scope:
1) All basic commands except 0Ch (Read Display Pixel Format), 36h (Memory Access Control) & 3Ah (Interface Pixel Format)
2) One supplementary command : B1h (OTP Write)

Note
(1) The RAM contents and other supplementary commands are unaffected by this command</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
</table>

9.3.3 Read Display Identification Information (04h)

<table>
<tr><th>04 h</th><th colspan="12">RDDIDIF (Read Display Identification Information)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>04</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>ID3</td><td>ID2</td><td>ID1</td><td>ID0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This read byte returns 4-bit Display Identification Information.

The 1st parameter is dummy read.
The 2nd parameter ID[3:0] returns the Display Identification Information burned in OTP through B1h command.</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value before OTP Programming</td><td>Default Value after OTP Programming</td></tr><tr><td>S/W Reset</td><td>ID[3:0] = 0000b</td><td>OTP content</td></tr><tr><td>H/W Reset</td><td>ID[3:0] = 0000b</td><td>OTP content</td></tr></table></td></tr>
</table>

9.3.4 Read Display Power Mode (0Ah)

<table>
<tr><th>0A h</th><th colspan="12">RDDPM (Read Display Power Mode)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0A</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>0</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
The 1st parameter is dummy read.

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>A5</td><td>Partial Mode ON/OFF</td></tr>
<tr><td>A4</td><td>Sleep In/Out</td></tr>
<tr><td>A3</td><td>Display Normal Mode ON/OFF</td></tr>
<tr><td>A2</td><td>All pixels OFF</td></tr>
</table>

• Bit A5 – Partial Mode ON/OFF (refer to command 12h)
‘0’ = Partial Mode OFF.
‘1’ = Partial Mode ON.

• Bit A4 – Sleep In/Out (refer to command 10h, 11h)
‘0’ = Sleep In Mode.
‘1’ = Sleep Out Mode.

• Bit A3 – Display Normal Mode ON/OFF (refer to command 13h)
‘0’ = Display Normal Mode OFF (i.e. Partial mode or vertical scroll mode enabled)
‘1’ = Display Normal Mode ON. (i.e. Neither partial mode nor vertical scroll mode enabled)

• Bit A2 – All pixels OFF (refer to command 28h, 29h)
‘0’ = All pixels OFF
‘1’ = Disable All pixels OFF</td></tr>
<tr><td>Command Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>S/W Reset</td><td>08h</td></tr>
<tr><td>H/W Reset</td><td>08h</td></tr>
</table>
</td></tr>
</table>

9.3.5 Read Display MADCTL (0Bh)

<table>
<tr><th>0B h</th><th colspan="12">RDDMADCTL (Read Display MADCTL)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0B</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>A7</td><td>A6</td><td>A5</td><td>0</td><td>A3</td><td>0</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
The 1st parameter is dummy read.
(MADCTL refers to command 36h Memory Access Control)

<table><tr><td>Bit</td><td>Description</td></tr><tr><td>A7</td><td>COM scan direction Remap</td></tr><tr><td>A6</td><td>Column Address Mapping</td></tr><tr><td>A5</td><td>Address Increment mode</td></tr><tr><td>A3</td><td>RGB Mapping</td></tr></table>
• Bit A7 – COM scan direction Remap
‘0’ = Scan from COM0 to COM[N –1] (When MADCTL A7=’0’).
‘1’ = Scan from COM[N-1] to COM0. (When MADCTL A7=’1’).
(Where N is the multiplex ratio.)

• Bit A6 – Column Address Mapping
‘0’ = Mapping display data RAM column 0 to SEG0 pin (When MADCTL A6=’0’).
‘1’ = Mapping display data RAM column 127 to SEG0 pin (When MADCTL A6=’1’).

• Bit A5 – Address Increment mode
‘0’ = Horizontal address increment mode (When MADCTL A5=’0’).
‘1’ = Vertical address increment mode (When MADCTL A5=’1’).

• Bit A3 – RGB Mapping
‘0’ = normal order SA,SB,SC (e.g. BGR) (When MADCTL A3=’0’).
‘1’ = reverse order SC,SB,SA (e.g. RGB) (When MADCTL A3=’1’).

Note
[1] Refer to section 9.3.26 Memory Access Control (36h).</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>S/W Reset</td><td>No Change</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

9.3.6 Read Display Pixel Format (0Ch)

<table>
<tr><th>0C h</th><th colspan="12">RDDCOLMOD (Read Display COLMOD)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0C</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A2</td><td>A1</td><td>A0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as described in the table below:
The 1st parameter is dummy read.

<table>
<tr><th>Bit</th><th>Description</th></tr>
<tr><td>A2</td><td rowspan="3">Control Interface Colour Format</td></tr>
<tr><td>A1</td></tr>
<tr><td>A0</td></tr>
</table>

• Bits A2, A1, A0 – Control Interface Colour Pixel Format Definition. See section “9.3.28 Interface Pixel Format (3Ah)”.

<table>
<tr><th>Interface Format</th><th>A2</th><th>A1</th><th>A0</th></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Not Defined</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Not Defined</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16 Bit/Pixel (65k color)</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18 Bit/Pixel (262k color)</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Not Defined</td><td>1</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>Command Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>18 bit/pixel</td></tr>
</table></td></tr>
</table>

9.3.7 Read Display Image Mode (0Dh)

<table>
<tr><th>0D h</th><th colspan="12">RDDIM (Read Display Image Mode)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0D</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>A7</td><td>0</td><td>A5</td><td>A4</td><td>0</td><td>0</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as below described:
The 1st parameter is dummy read.

• Bit A7 – Vertical Scrolling ON/OFF (refer to command 37h)
‘0’ = Vertical Scrolling is OFF.
‘1’ = Vertical Scrolling is ON.

• Bit A5 – Display Inversion ON/OFF (refer to command 20h & 21h)
‘0’ = Display Inversion is OFF.
‘1’ = Display Inversion is ON.

• Bit A4 – All Pixels ON (refer to command 23h &29h)
‘0’ = Disable All pixels ON
‘1’ = All pixels ON</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>S/W Reset</td><td>00h</td></tr><tr><td>H/W Reset</td><td>00h</td></tr></table></td></tr>
</table>

9.3.8 Read Display Signal Mode (0Eh)

<table>
<tr><th>0E h</th><th colspan="12">RDDSM (Read Display Signal Mode)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0E</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>A7</td><td>A6</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command indicates the current status of the display as below described:
The 1st parameter is dummy read.

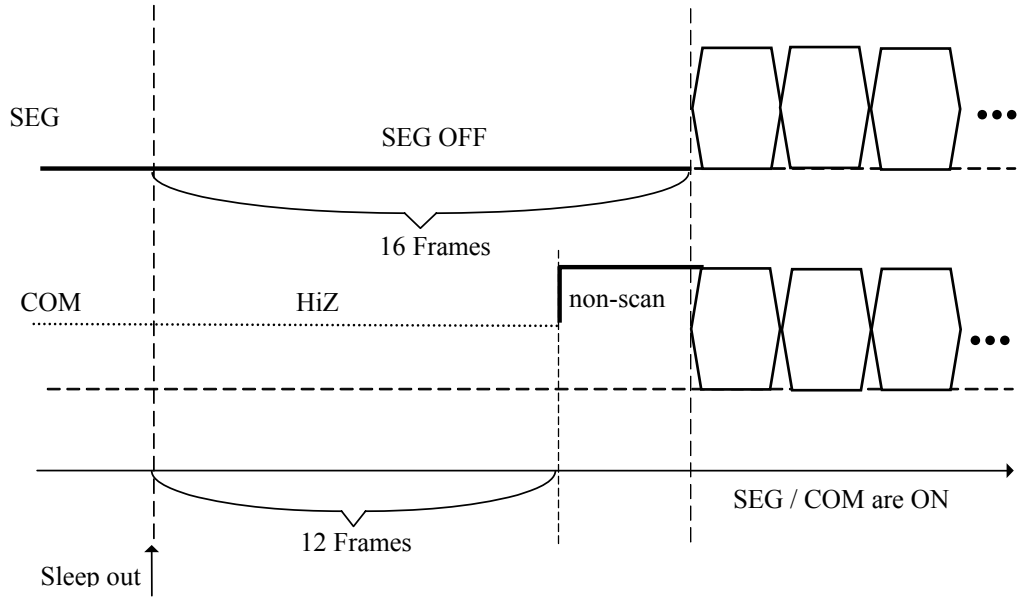
• Bit A7 – Tearing Effect Line ON/OFF (refer to command 34h, 35h)
‘0’ = Tearing Effect Line OFF.(i.e. output LOW)
‘1’ = Tearing Effect ON.

• Bit A6 – Tearing Effect Line Output Mode (refer to command 34h, 35h)
‘0’ = Mode 1.
‘1’ = Mode 2.</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>S/W Reset</td><td>A[7]=0</td></tr><tr><td>H/W Reset</td><td>A[7]=0</td></tr></table></td></tr>
</table>

9.3.9 Sleep In (10h)

<table>
<tr><th>10 h</th><th colspan="12">SLPIN (Sleep In)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>10</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to turn the OLED panel display OFF.
When the display is OFF, circuits will be turned OFF.
Internal V_{DD} regulator, MCU interface and memory are still working and the memory keeps its contents.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>S/W Reset</td><td>Sleep in mode</td></tr><tr><td>H/W Reset</td><td>Sleep in mode</td></tr></table></td></tr>
</table>

9.3.10 Sleep Out (11h)

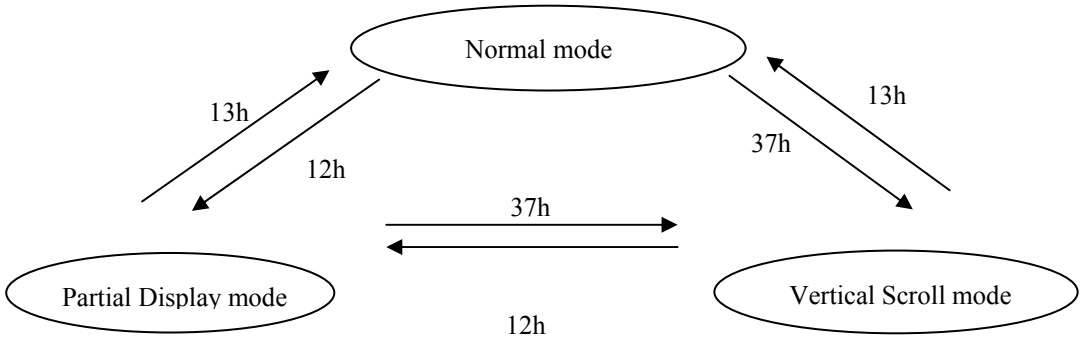
<table>
<tr><th>11 h</th><th colspan="12">SLPOUT (Sleep Out)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>11</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command turns ON the display and exist the sleep mode.
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when module is already in sleep out mode. Sleep Out mode can only be exit by the Sleep In Command (10h).</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>S/W Reset</td><td>Sleep in mode</td></tr><tr><td>H/W Reset</td><td>Sleep in mode</td></tr></table></td></tr>
</table>

9.3.11 Enable Partial Display (12h)

<table>
<tr><th>12 h</th><th colspan="12">PTLON (Enable Partial Display)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>12</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command turns ON partial mode. The partial mode window is described by the Set Partial Display Area command (30h).
To exit Partial mode, the Normal Display Mode ON command (13h) should be written.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Partial mode is active.</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>S/W Reset</td><td>Normal Mode ON</td></tr><tr><td>H/W Reset</td><td>Normal Mode ON</td></tr></table></td></tr>
</table>

9.3.12 Normal Display Mode ON (13h)

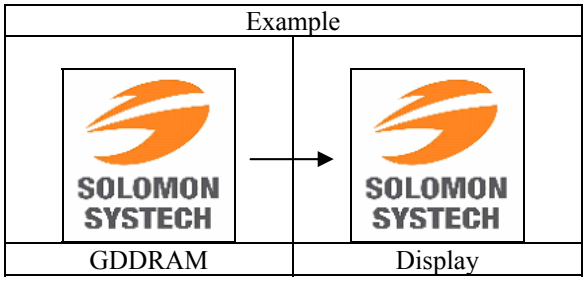
<table>
<tr><th>13 h</th><th colspan="12">NORON (Normal Display Mode ON)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>13</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command returns the display to normal mode.
Normal display mode ON means Partial Display mode OFF (1), Vertical Scroll mode OFF (2).

Figure 9-1 : Transition between different modes
 

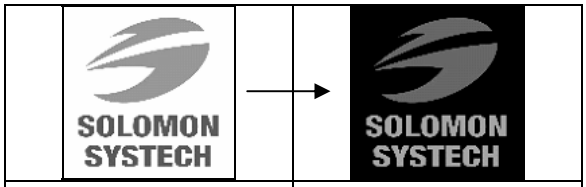
Note:
(1) Refer to command 12h for Partial Display mode
(2) Refer to command 37h for Vertical Scroll mode.</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when Normal Display mode is active.</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>S/W Reset</td><td>Normal Mode ON</td></tr><tr><td>H/W Reset</td><td>Normal Mode ON</td></tr></table></td></tr>
</table>

9.3.13 Display Inversion OFF (20h)

<table>
<tr><th>20 h</th><th colspan="12">INVOFF (Display Inversion OFF)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>20</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to recover from display inversion mode (21h).
This command makes no change of contents of RAM.

Figure 9-2 : Example of Inverse Display OFF
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when it is already in inversion OFF mode.</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>S/W Reset</td><td>Display Inversion OFF</td></tr><tr><td>H/W Reset</td><td>Display Inversion OFF</td></tr></table></td></tr>
</table>

9.3.14 Display Inversion ON (21h)

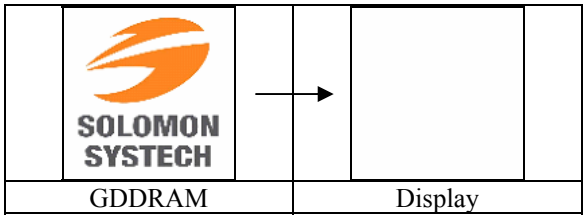
<table>
<tr><th>21 h</th><th colspan="12">INVON (Display Inversion ON)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enter into display inversion mode.
This command makes no change of contents of RAM. Every bit is inverted from the RAM to the display.
Figure 9-3 : Example of Inverse Display ON
 

GDDRAM | Display</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when it is already in inversion ON mode, All Pixels ON mode (23h) or All Pixels OFF mode (28h).</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>S/W Reset</td><td>Display Inversion OFF</td></tr><tr><td>H/W Reset</td><td>Display Inversion OFF</td></tr></table></td></tr>
</table>

9.3.15 All Pixels ON (23h)

<table>
<tr><th>23 h</th><th colspan="12">ALLPON (All Pixels ON)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>23</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command forces the entire display to be at “GS63” (1) regardless of the contents of the display data RAM

This command makes no change of contents of RAM.

Figure 9-4 : Example of all pixel ON
 

The display will exit the “All pixels ON” mode through issuing commands: ‘All Pixels OFF (28h)’, ’Disable All Pixels ON/OFF (29h)’ or ’Partial Mode ON (12h)(2)”.

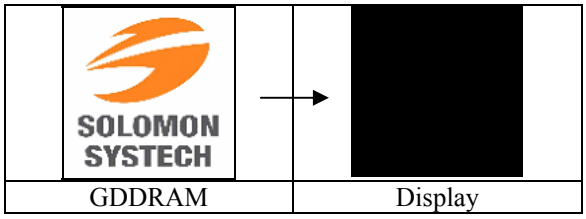
The display is showing the content of the RAM after’ Disable All Pixels ON/OFF (29h)’ and ’Partial Mode ON (12h)’.

Note
(1) Refer to section 8.8 for details of GS63
(2) The default partial display area is full MUX with 128RGB x 160, and the partial display area can be set by using command ‘Partial Area (30h)’</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when it is already in All Pixels ON mode.</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>S/W Reset</td><td>Disable All Pixels ON</td></tr><tr><td>H/W Reset</td><td>Disable All Pixels ON</td></tr></table></td></tr>
</table>

9.3.16 All Pixels OFF (28h)

<table>
<tr><th>28 h</th><th colspan="12">ALLPOFF (All Pixels OFF)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>28</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enter into ALL PIXELS OFF mode.
In this mode, the entire display to be at gray level “GS0” (1) regardless of the contents of the display data RAM.

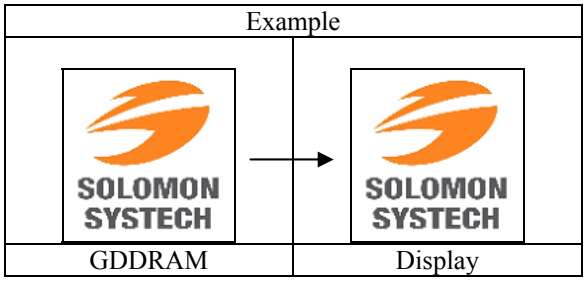
This command makes no change of contents of RAM.

Figure 9-5 : Example of all pixels OFF
 

The display returns to normal display (showing the content of the RAM) through issuing command 29h “Disable All Pixels ON/OFF”.

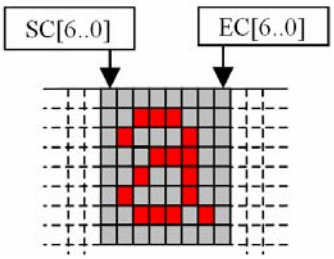
Note
(1) Refer to section 8.8 for details of GS0</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when it is already in display OFF mode.</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>S/W Reset</td><td>Disable All Pixels OFF</td></tr><tr><td>H/W Reset</td><td>Disable All Pixels OFF</td></tr></table></td></tr>
</table>

9.3.17 Disable All Pixels ON/OFF (29h)

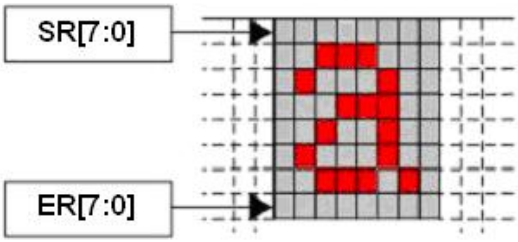
<table>
<tr><th>29 h</th><th colspan="11">DISPON (Display ON)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>29</td></tr>
<tr><td>Parameter</td><td colspan="12">NO PARAMETER</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to recover from All Pixels ON/OFF mode. Output from the RAM is enabled.
This command makes no change of contents of RAM.
Figure 9-6 : Example of Disable All Pixels ON/OFF
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">This command has no effect when it is already in Disable All Pixels ON/OFF mode.</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>S/W Reset</td><td>Disable All Pixels ON/OFF</td></tr><tr><td>H/W Reset</td><td>Disable All Pixels ON/OFF</td></tr></table></td></tr>
</table>

9.3.18 Set Column Address (2Ah)

<table>
<tr><th>2A h</th><th colspan="11">CASET (Set Column Address)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>2A</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>xx</td><td>SC6</td><td>SC5</td><td>SC4</td><td>SC3</td><td>SC2</td><td>SC1</td><td>SC0</td><td>00..7F</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>xx</td><td>EC6</td><td>EC5</td><td>EC4</td><td>EC3</td><td>EC2</td><td>EC1</td><td>EC0</td><td>00..7F</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to define area of RAM where MCU can access.

The values of Start Column Address (SC[6:0]) and End Column Address (EC[6:0]) are referred when Memory Write command (2Ch) is issued. Each value represents one column line in the RAM.
(Example)
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">SC[6:0] always must be equal to or less than EC[6:0]</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td colspan="2">Default Value</td></tr><tr><td rowspan="2">S/W Reset</td><td>When Bit A5 of command 36h = 0b</td><td>When Bit A5 of command 36h = 1b</td></tr><tr><td>SC[6:0]=00h
EC[6:0] = 7Fh</td><td>SC[6:0]=00h
EC[6:0] = 9Fh</td></tr><tr><td>H/W Reset</td><td>SC[6:0]=00h</td><td>EC[6:0] = 7Fh</td></tr></table></td></tr>
</table>

9.3.19 Set Row Address (2Bh)

<table>
<tr><th>2B h</th><th colspan="12">RASET (Set Row Address)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>2B</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>SR7</td><td>SR6</td><td>SR5</td><td>SR4</td><td>SR3</td><td>SR2</td><td>SR1</td><td>SR0</td><td>00..9F</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>ER7</td><td>ER6</td><td>ER5</td><td>ER4</td><td>ER3</td><td>ER2</td><td>ER1</td><td>ER0</td><td>00..9F</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to define area of RAM where MCU can access.
The values of Start row address (SR[7:0]) and End row address (ER[7:0]) are referred when Memory Write command (2Ch) is issued.
Each value represents one row line in the RAM.
(Example)
 
</td></tr>
<tr><td>Restriction</td><td colspan="12">SR[7:0] always must be equal to or less than ER[7:0]</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td colspan="2">Default Value</td></tr><tr><td rowspan="2">S/W Reset</td><td>When Bit A5 of command 36h = 0b</td><td>When Bit A5 of command 36h = 1b</td></tr><tr><td>SR[7:0] = 00h
ER[7:0] = 9Fh</td><td>SR[7:0] = 00h
ER[7:0] = 7Fh</td></tr><tr><td>H/W Reset</td><td>SR[7:0]=00h</td><td>ER[7:0] = 9Fh</td></tr></table></td></tr>
</table>

9.3.20 Memory Write (2Ch)

<table>
<tr><th>2C h</th><th colspan="12">RAMWR (Memory Write)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>2C</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>D17</td><td>D16</td><td>D15</td><td>D14</td><td>D13</td><td>D12</td><td>D11</td><td>D10</td><td>00..FF</td></tr>
<tr><td>:</td><td>1</td><td>1</td><td>↑</td><td>Dx7</td><td>Dx6</td><td>Dx5</td><td>Dx4</td><td>Dx3</td><td>Dx2</td><td>Dx1</td><td>Dx0</td><td>00..FF</td></tr>
<tr><td>Nth Parameter</td><td>1</td><td>1</td><td>↑</td><td>Dn7</td><td>Dn6</td><td>Dn5</td><td>Dn4</td><td>Dn3</td><td>Dn2</td><td>Dn1</td><td>Dn0</td><td>00..FF</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to transfer data from MCU to RAM.
After this command, data entries will be written into the display RAM until another command is written. (Sending any other command can stop memory write.) This command must be sent before write data into RAM.

When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.

Then parameters are stored in RAM and the column register and the row register incremented as stated in table below:

Table 9-1 : Controls for column and row counters under different conditions
<table><tr><th>Conditions</th><th>Column Counter</th><th>Row Counter</th></tr><tr><td>When RAMWR (Command 2Ch) / RAMRD (Command 2Eh) command is accepted.</td><td>Return to “Start Column”</td><td>Return to “Start Row”</td></tr><tr><td>Complete Pixel Read/Write action</td><td>Increment by 1</td><td>No change</td></tr><tr><td>The Column counter value is larger than “End column.”</td><td>Return to “Start Column”</td><td>Increment by 1</td></tr><tr><td>The Column counter value is larger than “End column” and the Row counter value is larger than “End Row”.</td><td>Return to “Start Column”</td><td>Return to “Start Row”</td></tr></table>
Refer to Table 8-8 for colour coding during write.</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

9.3.21 Memory Read (2Eh)

<table>
<tr><th>2E h</th><th colspan="12">RAMRD (Memory Read)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>2E</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>D17</td><td>D16</td><td>D15</td><td>D14</td><td>D13</td><td>D12</td><td>D11</td><td>D10</td><td>00..FF</td></tr>
<tr><td>:</td><td>1</td><td>↑</td><td>1</td><td>Dx7</td><td>Dx6</td><td>Dx5</td><td>Dx4</td><td>Dx3</td><td>Dx2</td><td>Dx1</td><td>Dx0</td><td>00..FF</td></tr>
<tr><td>(N+1) th Parameter</td><td>1</td><td>↑</td><td>1</td><td>Dn7</td><td>Dn6</td><td>Dn5</td><td>Dn4</td><td>Dn3</td><td>Dn2</td><td>Dn1</td><td>Dn0</td><td>00..FF</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to transfer data from RAM to MCU.
After this command, data is read from the display RAM until another command is written. (Sending any other command can stop memory read.) This command must be sent before read data from RAM.

When this command is accepted, the column register and the row register are reset to the Start Column/Start Row positions.

The 1st parameter is dummy read.
Then parameters are read back from the RAM .The column register and the row register incremented as in Table 9-1.

Refer to Table 8-9 for colour coding during read.

Note
(1) Memory Read is only possible via the Parallel Interface.</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>S/W Reset</td><td>Contents of memory is not cleared</td></tr><tr><td>H/W Reset</td><td>Contents of memory is not cleared</td></tr></table></td></tr>
</table>

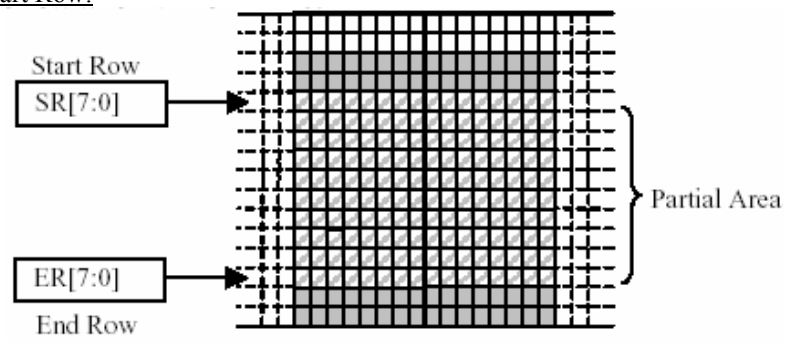
9.3.22 Partial Area (30h)

30 h	PLTAR (Partial Area)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	0	0	30
1st Parameter	1	1	↑	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	00..9F
2nd Parameter	1	1	↑	ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	00..9F

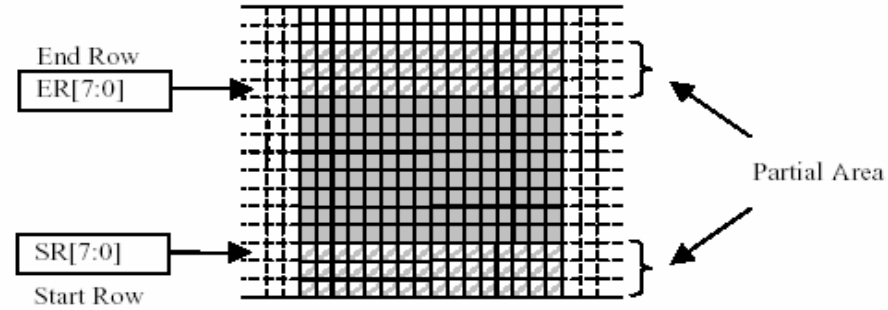
Description

This command defines the partial mode's display area. There are 2 parameters associated with this command, the first defines the Start Row (SR) and the second the End Row (ER), as illustrated in the figures below. SR and ER refer to the RAM Line Pointer.

If End Row>Start Row:

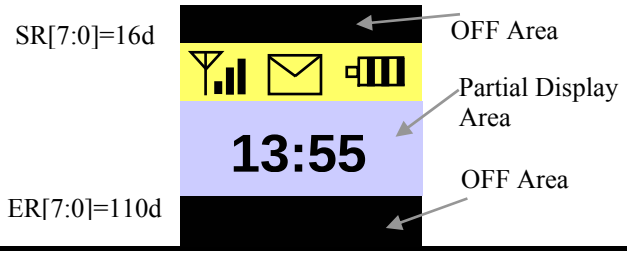


If End Row<Start Row:



If End Row = Start Row, then the Partial Area will be one row.

Figure 9-7 : Example of partial display function



Command Availability

Status	Availability
Normal Mode ON, Sleep Out	Yes
Partial Mode ON, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
S/W Reset	SR[7:0] =00h, ER[7:0]=9Fh
H/W Reset	SR[7:0] =00h, ER[7:0]=9Fh

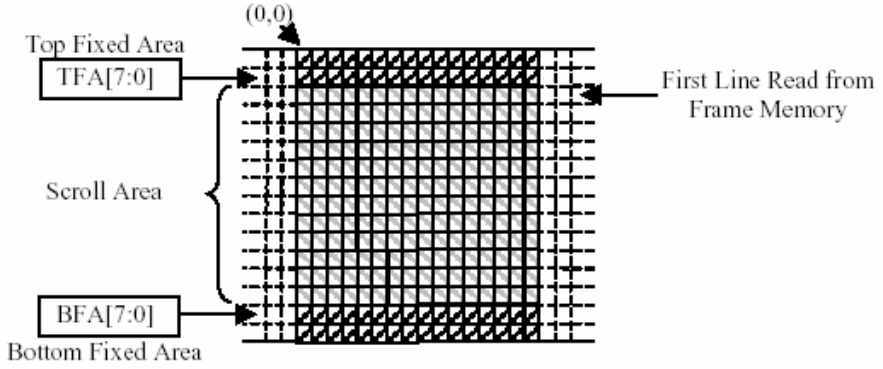
9.3.23 Vertical Scrolling Definition (33h)

33 h	VSCRDEF (Vertical Scrolling Definition)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	0	1	1	33
1st Parameter	1	1	↑	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0	00..A0
2nd Parameter	1	1	↑	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	00..A0
3rd Parameter	1	1	↑	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0	00..A0

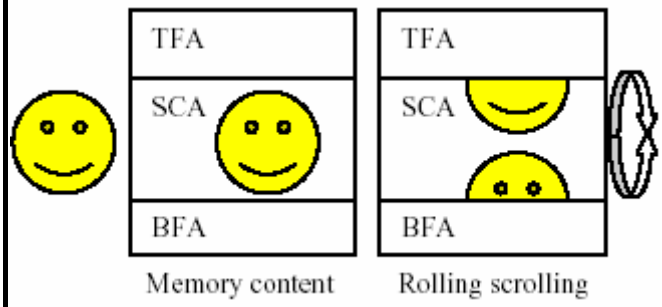
This command defines the Vertical Scrolling Area of the display. TFA, VSA and BFA refer to the RAM Line Pointer.

The 1st parameter TFA[7:0] describes the Top Fixed Area in number of rows.
The 2nd parameter VSA[7:0] describes the height of the Vertical Scrolling Area in number of rows from the Vertical Scrolling Start Address. The first row read from RAM appears immediately after the bottom most row of the Top Fixed Area.
The 3rd parameter BFA[7:0] describes the Bottom Fixed Area in number of rows. It should be set to MUX ratio - VSA - TFA. (where MUX ratio is set by command CAh).

i.e. TFA+VSA+BFA = MUX ratio



The vertical scrolling is determined by commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).



TFA = Top Fixed Area
SCA = Vertical Scrolling Area
BFA = Bottom Fixed Area

Command Availability

Status	Availability
Normal Mode ON, Sleep Out	Yes
Partial Mode ON, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value		
S/W Reset	TFA [7:0]=00h	VSA[7:0]=A0h	BFA[7:0]=00h
H/W Reset	TFA [7:0]=00h	VSA[7:0]=A0h	BFA[7:0]=00h

9.3.24 Disable Tearing Effect (34h)

34 h	TEOFF (Tearing Effect Line OFF)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	0	0	34
Parameter	NO PARAMETER											
Description	This command is used to turn OFF (output LOW) the Tearing Effect output signal from the TE signal line.											
Restriction	This command has no effect when Tearing Effect output is already OFF.											
Command Availability												

Status	Availability
Normal Mode ON, Sleep Out	Yes
Partial Mode ON, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
S/W Reset	OFF
H/W Reset	OFF

9.3.25 Enable Tearing Effect (35h)

35 h	TEON (Tearing Effect Line ON)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	0	1	35
Parameter	1	1	↑	xx	xx	xx	xx	xx	xx	xx	M0	xx
Description	This command is used to turn ON the Tearing Effect output signal from the TE signal line. The Tearing Effect Line ON has one parameter which describes the mode of the Tearing Effect Output Line. When M[0]=0: Vertical synchronization (Vsync) pulse only When M[0]=1: Vertical synchronization (Vsync) pulse + Horizontal synchronization (Hsync) pulse Refer to Section 8.10 for details.											
Command Availability												

Status	Availability
Normal Mode ON, Sleep Out	Yes
Partial Mode ON, Sleep Out	Yes
Sleep In	Yes

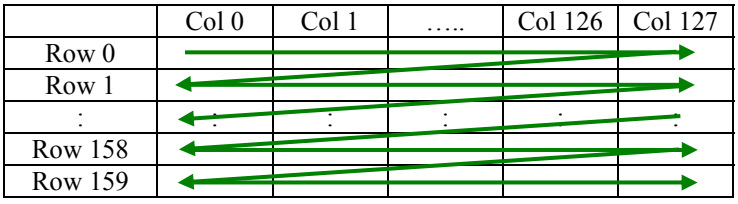
Default

Status	Default Value
S/W Reset	OFF
H/W Reset	OFF

9.3.26 Memory Access Control (36h)

<table>
<tr><th>36 h</th><th colspan="12">MADCTL (Memory Access Control)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>36</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>A7</td><td>A6</td><td>A5</td><td>0</td><td>A3</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>1</td><td>↑</td><td>xx</td><td>xx</td><td>BS3</td><td>BS2</td><td>xx</td><td>xx</td><td>A1</td><td>A0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command has multiple configurations, for example, defines read/write scanning direction of RAM , MCU bus interface selection bits and COM pins hardware configuration. Each bit setting is described as follows:
<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>A7</td><td>COM scan direction Remap</td><td rowspan="3">Details refer to description below.</td></tr>
<tr><td>A6</td><td>Column Address Mapping</td></tr>
<tr><td>A5</td><td>Address Increment mode</td></tr>
<tr><td>A3</td><td>RGB Mapping</td><td>This command bit is made for flexible layout of segment signals in OLED module to match filter design.

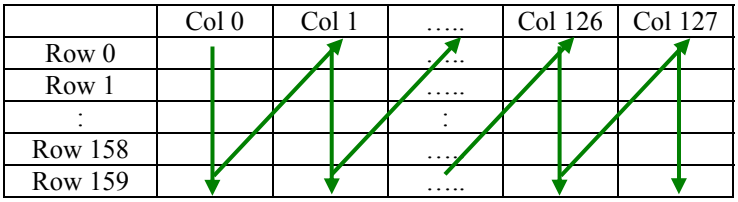
A[3]=0, normal order SA,SB,SC (e.g. BGR) [reset]
A[3]=1, reverse order SC,SB,SA (e.g. RGB)</td></tr>
<tr><td>A1</td><td>COM Left / Right Remap</td><td>This command bit is made for flexible layout of common signals in OLED module with COM0 arranged on either left or right side.

A[1]=0, Disable left-right swapping on COM [reset]
A[1]=1, Set left-right swapping on COM</td></tr>
<tr><td>A0</td><td>Odd Even Split of COM pins</td><td>This bit can set the odd even arrangement of COM pins.
A[0] = 0: Disable COM split odd even, pin assignment of common is in sequential.
A[0] = 1: Enable COM split odd even, pin assignment of common is in odd even split. [reset]</td></tr>
<tr><td>BS[3:2]</td><td>MCU bus interface selection bits</td><td>Select appropriate logic setting as described in the following table.
<table>
<tr><th>BS[3:2]</th><th>Interface</th></tr>
<tr><td>00</td><td>SPI, 8-bit parallel [reset]</td></tr>
<tr><td>01</td><td>16-bit parallel</td></tr>
<tr><td>11</td><td>18-bit parallel</td></tr>
</table>
BS3 and BS2 are command programmable (by command 36h).
BS1 and BS0 are pin select (refer to Table 7-2).</td></tr>
</table>
Address increment mode (A[5])
When it is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read/written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 9-8.
Figure 9-8 : Address Pointer Movement of Horizontal Address Increment Mode

</td></tr>
</table>

36 h	MADCTL (Memory Access Control)

When A[5] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read/written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 9-9.

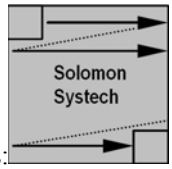
Figure 9-9 : Address Pointer Movement of Vertical Address Increment Mode

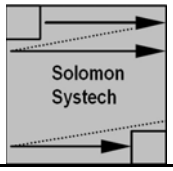
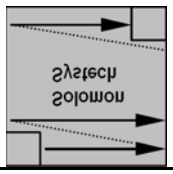
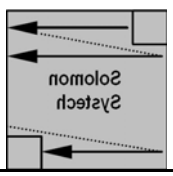


- Column Address Mapping (A[6])
  This command bit is made for flexible layout of segment signals in OLED module with segment arranged from left to right or vice versa. The display direction is either mapping display data RAM column 0 to SEG0 pin (A[6] = 0), or mapping display data RAM column 127 to SEG0 pin (A[6] = 1). The effects of both are shown in Figure 9-10.

- COM scan direction Remap (A[7])
  This bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa. Details of bit A[7] can be found in Figure 9-10.
  A[7]=0, Scan from COM0 to COM[N –1] (No Remap)
  A[7]=1, Scan from COM[N-1] to COM0 (Remap). Where N is the multiplex ratio.

Figure 9-10 : Example Bit A[5], A[6], A[7] in command MADCTL (36h)

Example square image is like this: 

Display Example	A5	A6	A7
Normal 	0	0	0
Y-Invert 	0	0	1
X-Invert 	0	1	0

36 h	MADCTL (Memory Access Control)

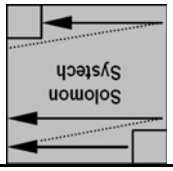
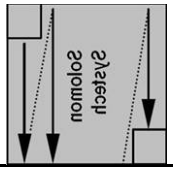
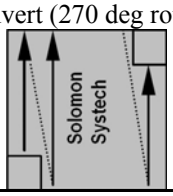
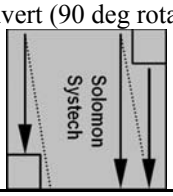
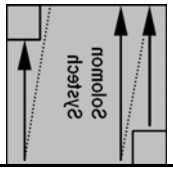
Display Example	A5	A6	A7
X-Invert+ Y-Invert 	0	1	1
Exchange Row-Column 	1	0	0
Exchange Row-Column + X Invert (270 deg rotation) 	1	0	1
Exchange Row-Column + Y Invert (90 deg rotation) 	1	1	0
Exchange Row-Column + X Invert + Y Invert 	1	1	1

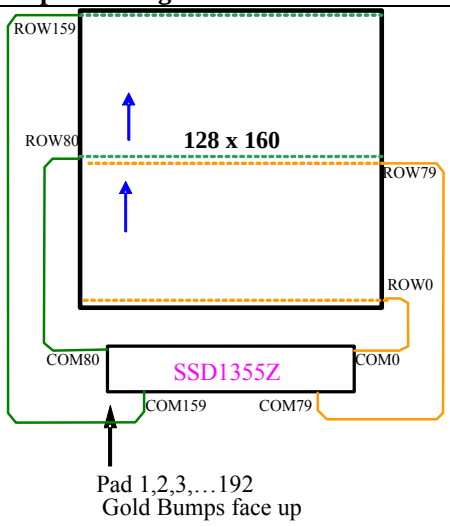
Figure 9-11 : COM Pins Hardware Configuration (MUX ratio: 160)

Case and Conditions	COM pins Configurations

A

A[0] =0	A[1]=0	A[7]=0
Disable Odd Even Split of COM pins	Disable COM Left / Right Remap	COM Scan Direction : from COM0 to COM159

Pin name	Panel
COM 0	Row 0
COM 1	Row 1
COM 2	Row 2
… …	… …
COM 78	Row 78
COM 79	Row 79
COM 80	Row 80
COM 81	Row 81
…	… …
COM 157	Row 157
COM 158	Row 158
COM 159	Row 159



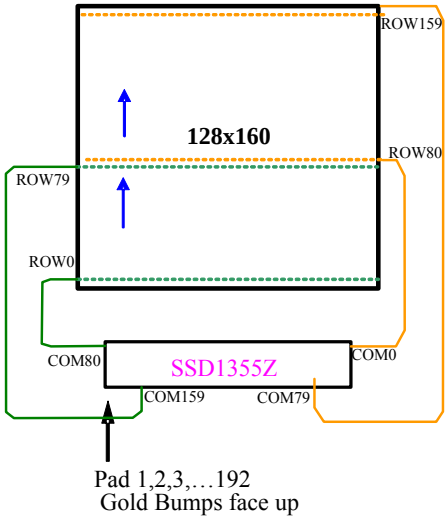
36 h	MADCTL (Memory Access Control)

Case and Conditions | **COM pins Configurations**

B

A[0] =0	A[1]=1	A[7]=0
Disable Odd Even Split of COM pins	Enable COM Left / Right Remap	COM Scan Direction : from COM0 to COM159

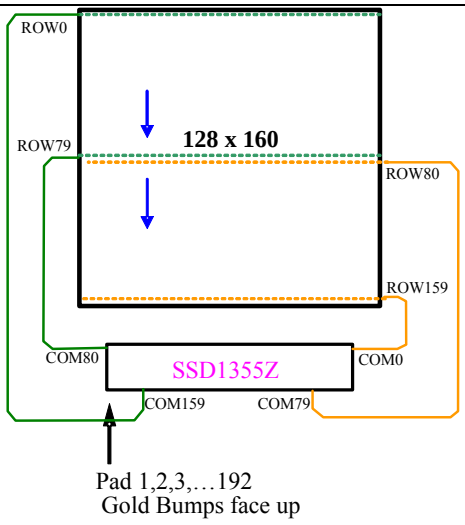
Pin name	Panel
COM 0	Row 80
COM 1	Row 81
COM 2	Row 82
… …	… …
COM 78	Row 158
COM 79	Row 159
COM 80	Row 0
COM 81	Row 1
…	… …
COM 157	Row 77
COM 158	Row 78
COM 159	Row 79



C

A[0] =0	A[1]=0	A[7]=1
Disable Odd Even Split of COM pins	Disable COM Left / Right Remap	COM Scan Direction : from COM159 to COM0

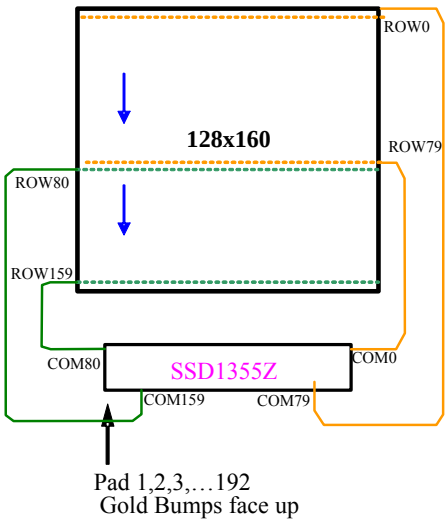
Pin name	Panel
COM 0	Row 159
COM 1	Row 158
COM 2	Row 157
… …	… …
COM 78	Row 81
COM 79	Row 80
COM 80	Row 79
COM 81	Row 78
…	… …
COM 157	Row 2
COM 158	Row 1
COM 159	Row 0



D

A[0] =0	A[1]=1	A[7]=1
Disable Odd Even Split of COM pins	Enable COM Left / Right Remap	COM Scan Direction : from COM159 to COM0

Pin name	Panel
COM 0	Row 79
COM 1	Row 78
COM 2	Row 77
… …	… …
COM 78	Row 1
COM 79	Row 0
COM 80	Row 159
COM 81	Row 158
…	… …
COM 157	Row 82
COM 158	Row 81
COM 159	Row 80



36 h	MADCTL (Memory Access Control)

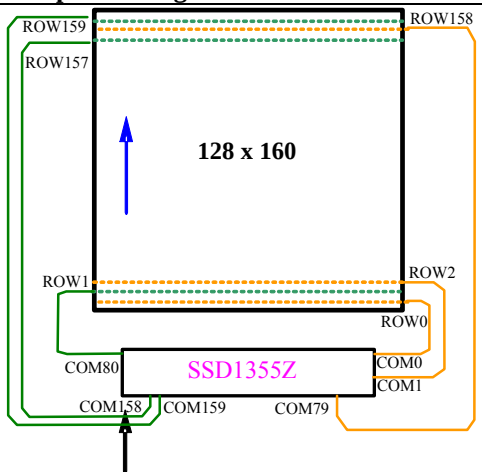
Case and Conditions

E [reset]

A[0] =1	A[1]=0	A[7]=0
Enable Odd Even Split of COM pins	Disable COM Left / Right Remap	COM Scan Direction : from COM0 to COM159

Pin name	Panel
COM 0	Row 0
COM 1	Row 2
COM 2	Row 4
… …	… …
COM 78	Row 156
COM 79	Row 158
COM 80	Row 1
COM 81	Row 3
…	… …
COM 157	Row 155
COM 158	Row 157
COM 159	Row 159

COM pins Configurations

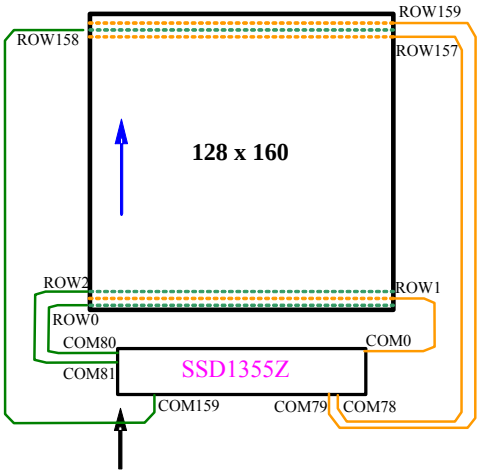


Pad 1,2,3,…192
Gold Bumps face up

F

A[0] =1	A[1]=1	A[7]=0
Enable Odd Even Split of COM pins	Enable COM Left / Right Remap	COM Scan Direction : from COM0 to COM159

Pin name	Panel
COM 0	Row 1
COM 1	Row 3
COM 2	Row 5
… …	… …
COM 78	Row 157
COM 79	Row 159
COM 80	Row 0
COM 81	Row 2
…	… …
COM 157	Row 154
COM 158	Row 156
COM 159	Row 158

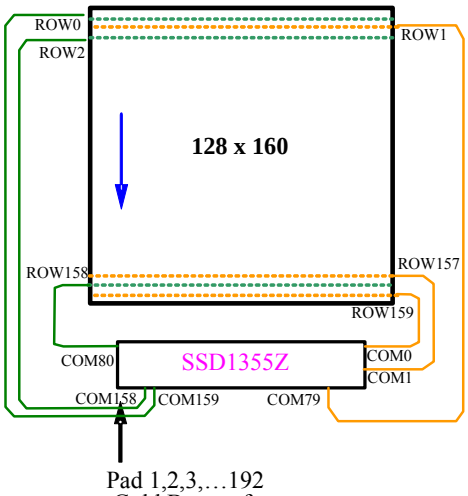


Pad 1,2,3,…192
Gold Bumps face up

G

A[0] =1	A[1]=0	A[7]=1
Enable Odd Even Split of COM pins	Disable COM Left / Right Remap	COM Scan Direction : from COM159 to COM0

Pin name	Panel
COM 0	Row 159
COM 1	Row 157
COM 2	Row 155
… …	… …
COM 78	Row 3
COM 79	Row 1
COM 80	Row 158
COM 81	Row 156
…	… …
COM 157	Row 4
COM 158	Row 2
COM 159	Row 0



Pad 1,2,3,…192
Gold Bumps face up

36 h	MADCTL (Memory Access Control)

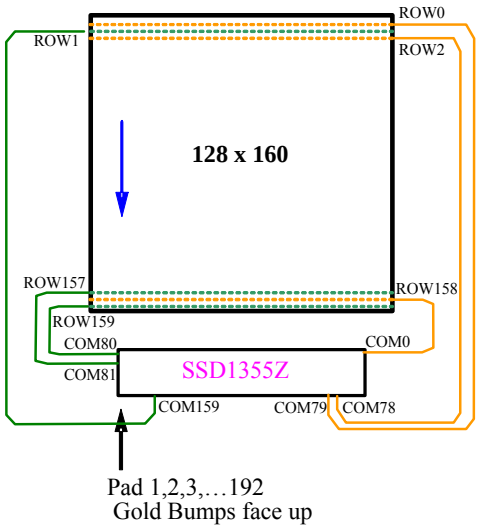
Case and Conditions

H

A[0] =1	A[1]=1	A[7]=1
Enable Odd Even Split of COM pins	Enable COM Left / Right Remap	COM Scan Direction : from COM159 to COM0

Pin name	Panel
COM 0	Row 158
COM 1	Row 156
COM 2	Row 154
… …	… …
COM 78	Row 2
COM 79	Row 0
COM 80	Row 159
COM 81	Row 157
…	… …
COM 157	Row 5
COM 158	Row 3
COM 159	Row 1

COM pins Configurations



Command Availability

Status	Availability
Normal Mode ON, Sleep Out	Yes
Partial Mode ON, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
S/W Reset	No Change
H/W Reset	A7=0, A6=0, A5=0, A4=0, A3=0, A1=0, A0=1 BS[3:2]=00.

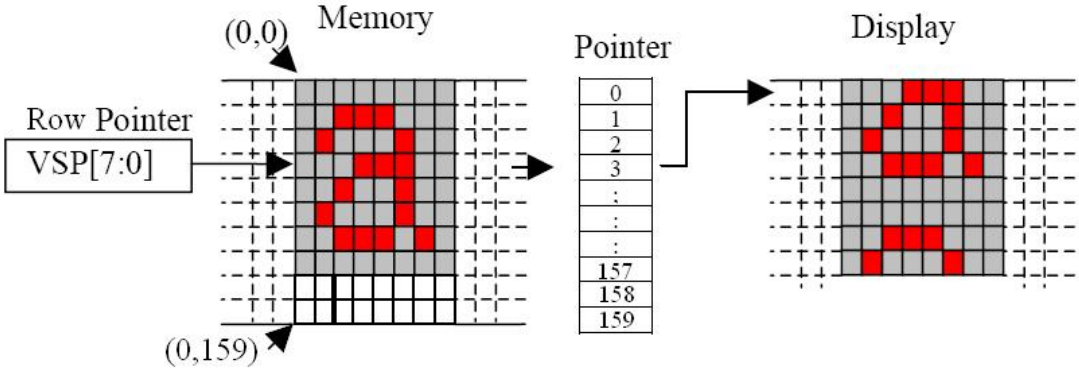
9.3.27 Vertical Scrolling Start Address (37h)

37 h	VSCRSADD (Vertical Scrolling Start Address)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	0	0	1	1	0	1	1	1	37
Parameter	1	1	↑	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0	00..23

Description

This command is used together with Vertical Scrolling Definition (33h). These two commands describe the scrolling area and the scrolling mode.
The Vertical Scrolling Start Address command has one parameter which describes the address of the row in the RAM that will be written as the first row after the last row of the Top Fixed Area on the display as illustrated below:

Example:
When Top Fixed Area = Bottom Fixed Area = 0, Vertical Scrolling Area = 160 and VSP='3'.



Note
(1) When new Pointer position and Picture Data are sent, the result on the display will happen at the next frame to avoid tearing effect.
(2) VSP refers to the RAM row Pointer.
(3) Vertical Scroll mode is entered by issuing this command. Entering command 13h can OFF Vertical Scroll mode.

Restriction

Since the value of the Vertical Scrolling Start Address is absolute (with reference to the RAM), it must not enter the fixed area (defined by Vertical Scrolling Definition (33h), otherwise undesirable image will be displayed on the Panel.

e.g.
If Top Fixed Area =2, Bottom Fixed Area = 3, Vertical Scrolling Area = 155 (set by command 33h), then RAM row 0, row 1, row 157, row 158 and row 159 are in the fixed area.
As a result VSP should be set within the range 2~156.

Command Availability

Status	Availability
Normal Mode ON, Sleep Out	Yes
Partial Mode ON, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
S/W Reset	VSP[7:0]=00h
H/W Reset	VSP[7:0]=00h

9.3.28 Interface Pixel Format (3Ah)

<table>
<tr><th>3A h</th><th colspan="11">COLMOD (Interface Pixel Format)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>3A</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>XX</td><td>XX</td><td>XX</td><td>XX</td><td>XX</td><td>A2</td><td>A1</td><td>A0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to define the format of RGB picture data, which is to be transferred via the MCU Interface. The formats are shown in the table:

<table>
<tr><th>Interface Format</th><th>A2</th><th>A1</th><th>A0</th></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Not Defined</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Not Defined</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Not Defined</td><td>0</td><td>1</td><td>1</td></tr>
<tr><td>Not Defined</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>16 Bit/Pixel (65k color)</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>18 Bit/Pixel (262k color)</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>Not Defined</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Note
(1) 16 Bit/Pixel mode is not available for 18bit interface.</td></tr>
<tr><td>Command Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>S/W Reset</td><td>No Change</td></tr>
<tr><td>H/W Reset</td><td>18 Bit/Pixel</td></tr>
</table></td></tr>
</table>

9.3.29 Write Luminance (51h)

This command has combined effect with the High Power Protection function. To eliminate the effect, once may set according to below instruction.

Before setting write luminance command, disable the High Power protection (command: B3h → 00h or 01h) first.

e.g. Disable High Power Protection -> set luminance to 1111b

B3h→ 00h or 01h → 51h → F0h.

"00" or "01" depends on enable/disable internal V_{DD} regulator.

<table>
<tr><th>51 h</th><th colspan="12">WRLUM (Write Luminance)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>51</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>LUM3</td><td>LUM2</td><td>LUM1</td><td>LUM0</td><td>XX</td><td>XX</td><td>XX</td><td>XX</td><td>00..FF</td></tr>
<tr><td>Description</td><td colspan="12">This command is to control the segment output current by a scaling factor. This factor is common to color A, B and C. The chip has 16 master control steps. The factor is ranged from 1 [0000b] to 16 [1111b]. Reset is 16 [1111b]. The smaller the master current value, the dimmer the OLED panel display is set.
<table>
<tr><th>LUM[3:0]</th><th>Master Current Control</th></tr>
<tr><td>0000</td><td>1/16</td></tr>
<tr><td>0001</td><td>2/16</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>1110</td><td>15/16</td></tr>
<tr><td>1111</td><td>16/16</td></tr>
</table></td></tr>
<tr><td>Command Availability</td><td colspan="12">
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Partial Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>S/W Reset</td><td>LUM[3:0]=1111</td></tr>
<tr><td>H/W Reset</td><td>LUM[3:0]=1111</td></tr>
</table></td></tr>
</table>

9.3.30 Read Luminance Value (52h)

<table>
<tr><th>52 h</th><th colspan="12">RDLUM (Read Luminance Value)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>52</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>↑</td><td>1</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>2nd Parameter</td><td>1</td><td>↑</td><td>1</td><td>LUM3</td><td>LUM2</td><td>LUM1</td><td>LUM0</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This read byte returns 4-bit master current value set by command 51h.

The 1st parameter is dummy read.
The 2nd parameter LUM[3:0] returns the 4-bit master current value set by command 51h.</td></tr>
<tr><td>Command Availability</td><td colspan="12"><table><tr><td>Status</td><td>Availability</td></tr><tr><td>Normal Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Partial Mode ON, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>S/W Reset</td><td>F0h</td></tr><tr><td>H/W Reset</td><td>F0h</td></tr></table></td></tr>
</table>

9.3.31 Read Display Identification Information (DAh)

DA h	RDDIDIF (Read Display Identification Information)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	1	1	0	1	0	DA
1st Parameter	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd Parameter	1	↑	1	0	0	0	0	ID3	ID2	ID1	ID0	xx
Description	This command performs the same function as command 04h This read byte returns 4-bit Display Identification Information. The 1st parameter is dummy read. The 2nd parameter ID[3:0] returns the Display Identification Information burned in OTP through B1h command.											
Command Availability												
Default												

Status	Availability
Normal Mode ON, Sleep Out	Yes
Partial Mode ON, Sleep Out	Yes
Sleep In	Yes

Status	Default Value before OTP Programming	Default Value after OTP Programming
S/W Reset	ID[3:0] = 0000b	OTP content
H/W Reset	ID[3:0] = 0000b	OTP content

9.3.32 OTP Write (B1h)

B1 h	OTPWR (OTP Write)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	0	0	1	B1
1st Parameter	1	1	↑	P7	P6	P5	P4	P3	P2	P1	P0	xx
2nd Parameter	1	1	↑	CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	xx
3rd Parameter	1	1	↑	ID3	ID2	ID1	ID0	CC3	CC2	CC1	CC0	xx

Description

This command is used to program data from MCU to OTP (One Time Program).

The 1st parameter P[7:0] is used to select between OTP programming or OTP Emulation:

Function	P[7:0]
OTP Programming : Burn the OTP contents	2Bh
OTP Emulation : For evaluation purpose The emulated OTP bytes can be cleared by hardware or software reset (01h)	2Eh

The 2nd and 3rd parameters are for the OTP bytes:

- ID[3:0] is for the Display Identification Information. The burned Display Identification Information can be read through 04h , B2h or DAh.
- CA[3:0] is for trimming Color A contrast (1)
- CB[3:0] is for trimming Color B contrast (1)
- CC[3:0] is for trimming Color C contrast (1)

Table 9-2 : Colour contrast adjustment

CA [3:0]	Adjustment	CB [3:0]	Adjustment	CC [3:0]	Adjustment
0000	0%	0000	0%	0000	0%
0001	+1/32	0001	+1/32	0001	+1/32
0010	+2/32	0010	+2/32	0010	+2/32
0011	+3/32	0011	+3/32	0011	+3/32
0100	+4/32	0100	+4/32	0100	+4/32
0101	+5/32	0101	+5/32	0101	+5/32
0110	+6/32	0110	+6/32	0110	+6/32
0111	+7/32	0111	+7/32	0111	+7/32
1000	0%	1000	0%	1000	0%
1001	-1/32	1001	-1/32	1001	-1/32
1010	-2/32	1010	-2/32	1010	-2/32
1011	-3/32	1011	-3/32	1011	-3/32
1100	-4/32	1100	-4/32	1100	-4/32
1101	-5/32	1101	-5/32	1101	-5/32
1110	-6/32	1110	-6/32	1110	-6/32
1111	-7/32	1111	-7/32	1111	-7/32

The steps for OTP programming (P[7:0]=2Bh):

1. Power up V_{PP} to 2.5V
2. Power up V_{DD} to 2.5V
3. Hardware Reset
4. Set DCLK frequency to 9kHz (2) , (3)
5. Send OTP write Command B1h
6. Send Data 2Bh for OTP burn
7. Power Up V_{PP} to 7.5V
8. Send two OTP bytes through MCU interface
9. Wait >=1ms for OTP burn process
10. Lower V_{PP} and wait for V_{PP} down to 2.5V
11. Send Software Reset Command 01h to exit OTP programming
12. Wait >= 10us
13. Power OFF V_{DD}
14. Power OFF V_{PP}

<table>
<tr><th>B1 h</th><th>OTPWR (OTP Write)</th></tr>
<tr><td></td><td>The steps for OTP Emulation (P[7:0]=2Eh):
1. Send OTP write Command B1h
2. Send Data 2Eh for OTP Emulation
3. Send two OTP bytes through MCU interface
4. Hardware reset or Send Command 01h Software Reset to exit OTP programming

Note
(1) The contrast of color A, B, C are set by command BAh, BBh and BCh respectively. The adjusted contrast values (i.e. after trimming) are subject to the boundary and resolution in BAh, BBh and BCh.
(2) Use the following command sequence to set DCLK frequency to 9kFz :Command FDh, Data B3h, Command D2h, Data 67h.
(3) If External CL clock is used, the CL frequency should be set > 200kHz and set DCLK = 9kHz (7~11kHz)</td></tr>
<tr><td>Default</td><td><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>S/W Reset</td><td>N/A</td></tr><tr><td>H/W Reset</td><td>N/A</td></tr></table></td></tr>
</table>

9.3.33 OTP MCU Read (B2h)

B2 h	OTPRD (OTP MCU Read)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	0	1	0	B2
1st Parameter	1	↑	1	xx	xx	xx	xx	xx	xx	xx	xx	xx
2nd Parameter	1	↑	1	CB3	CB2	CB1	CB0	CA3	CA2	CA1	CA0	xx
3rd Parameter	1	↑	1	ID3	ID2	ID1	ID0	CC3	CC2	CC1	CC0	xx
Description	This command is used to transfer data from OTP to MCU. The 1st parameter is dummy read. The next 2 bytes read parameters are OTP contents burned through B1h. The D/C# pin is set to high for reading parameters.											
Default	Status: H/W Reset — Default Value: N/A											

9.3.34 Function Selection (B3h)

B3 h	FUSEL (Function Selection)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	0	0	1	1	B3
Parameter	1	1	↑	0	A6	0	0	0	0	A1	A0	02..03
Description	This command is used to set the internal V_{DD} Regulator. • Bit A0 – Internal V_{DD} Regulator Selection '0' = Select external V_{DD} '1' = Enable internal V_{DD} regulator [reset] • Bit A1 – High Power Protection Selection '0' = Disable high power protection '1' = Enable high power protection [reset] • Bit A6 – I_{REF} Selection '0' = Select external I_{REF} [reset] '1' = Enable internal I_{REF}											
Default	Status: H/W Reset — Default Value: A0=1b, A1=1b, A6=0b											

9.3.35 Linear Gamma Look Up Table (B9h)

<table>
<tr><th>B9 h</th><th colspan="12">LINGLUT (Linear Gamma Look Up Table)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>B9</td></tr>
<tr><td>Parameter</td><td colspan="12">no parameter</td></tr>
<tr><td>Description</td><td colspan="12">Reset built in Linear Gray Scale table

GS0 = Gamma Setting 0;
GS1 = Gamma Setting 2
GS2 = Gamma Setting 4;
GS3 = Gamma Setting 6;
:
GS31 = Gamma Setting 62
GS32 = Gamma Setting 65;
GS33 = Gamma Setting 67;
:
GS62 = Gamma Setting 125;
GS63 = Gamma Setting 127;

Refer to Section 8.8 for details.</td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>H/W Reset</td><td>Linear Gamma Look UP Table</td></tr></table></td></tr>
</table>

9.3.36 Set Contrast For Color A, B &C (BAh)

<table>
<tr><th>BA h</th><th colspan="12">ISEGABC(Set Contrast For Color A, B & C)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>BA</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>xx</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>BB</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td>xx</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>BC</td></tr>
<tr><td>Parameter</td><td>1</td><td>1</td><td>↑</td><td>C7</td><td>C6</td><td>C5</td><td>C4</td><td>C3</td><td>C2</td><td>C1</td><td>C0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">A[7:0] : Set contrast for all color "A" segment (Pins :SA0 – SA127)
B[7:0] : Set contrast for all color "B" segment (Pins :SB0 – SB127)
C[7:0] : Set contrast for all color "C" segment (Pins :SC0 – SC127)

Note
(1) All six bytes (BAh A[7:0], BBh B[7:0] and BCh C[7:0]) must be inputted together. For example: the original value is like that
<table>
<tr><td colspan="2">Original value</td></tr>
<tr><td>BAh A[7:0]:</td><td>80h</td></tr>
<tr><td>BBh B[7:0]:</td><td>80h</td></tr>
<tr><td>BCh C[7:0]:</td><td>80h</td></tr>
</table>
If once wanted to change the value of BBh B[7:0] to 75h, then all the following 6 bytes must be inputted as:
BAh (command), 80h (data),
BBh (command), 75h (data),
BCh (command), 80h (data).
Otherwise, the changes may not be activated.</td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>H/W Reset</td><td>A[7:0]=128d (80h)
B[7:0]=128d (80h)
C[7:0]=128d (80h)</td></tr>
</table>
</td></tr>
</table>

9.3.37 Set First Pre-Charge Voltage (BDh)

<table>
<tr><th>BD h</th><th colspan="12">VPSET (Set First Pre-Charge Voltage)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>BD</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>xx</td><td>xx</td><td>xx</td><td>V4</td><td>V3</td><td>V2</td><td>V1</td><td>V0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to set the first pre-charge voltage for the three colors as follow:
<table>
<tr><td>V[4:0]</td><td>Voltage pre-charge for three colors</td></tr>
<tr><td>00000</td><td>0.2* V_{CC}</td></tr>
<tr><td>:</td><td>:</td></tr>
<tr><td>11111</td><td>0.6* V_{CC}</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>H/W Reset</td><td>V[4:0]=10111b</td></tr>
</table></td></tr>
</table>

9.3.38 Gamma Look Up Table (BEh)

BE h	GLUT (Gamma Look Up Table)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	0	1	1	1	1	1	0	BE
1st Parameter	1	1	↑	xx	$A01_6$	$A01_5$	$A01_4$	$A01_3$	$A01_2$	$A01_1$	$A01_0$	xx
:	1	1	↑	xx	Ann_6	Ann_5	Ann_4	Ann_3	Ann_2	Ann_1	Ann_0	xx
32nd Parameter	1	1	↑	xx	$A32_6$	$A32_5$	$A32_4$	$A32_3$	$A32_2$	$A32_1$	$A32_0$	xx
33rd Parameter	1	1	↑	xx	$B01_6$	$B01_5$	$B01_4$	$B01_3$	$B01_2$	$B01_1$	$B01_0$	xx
:	1	1	↑	xx	Bnn_6	Bnn_5	Bnn_4	Bnn_3	Bnn_2	Bnn_1	Bnn_0	xx
64th Parameter	1	1	↑	xx	$B32_6$	$B32_5$	$B32_4$	$B32_3$	$B32_2$	$B32_1$	$B32_0$	xx
65th Parameter	1	1	↑	xx	$C01_6$	$C01_5$	$C01_4$	$C01_3$	$C01_2$	$C01_1$	$C01_0$	xx
:	1	1	↑	xx	Cnn_6	Cnn_5	Cnn_4	Cnn_3	Cnn_2	Cnn_1	Cnn_0	xx
96th Parameter	1	1	↑	xx	$C32_6$	$C32_5$	$C32_4$	$C32_3$	$C32_2$	$C32_1$	$C32_0$	xx
Description	This command is used to define three programmable gamma look-up tables for color A, B and C respectively in terms of Gray Scale (GS). Except GS0, which is zero as it has no pre-charge and current drive, each entry GS level is programmed in the Gamma Setting. The larger value of Gamma Setting, the brighter is the OLED pixel when it's turned ON. Refer to Section 8.8 for details. Following the command BEh, the Gamma Setting for GS1, GS3, GS5, …, GS61, GS63 should be set one by one in sequence for color A, B and C: (1) A01[6:0] / B01[6:0] / C01[6:0]: Gamma Setting for GS1 of color A / B / C respectively ; A02[6:0] / B02[6:0] / C02[6:0]: Gamma Setting for GS3 of color A / B / C respectively ; A03[6:0] / B03[6:0] / C03[6:0]: Gamma Setting for GS5 of color A / B / C respectively ; A04[6:0] / B04[6:0] / C04[6:0]: Gamma Setting for GS7 of color A / B / C respectively ; A05[6:0] / B05[6:0] / C05[6:0]: Gamma Setting for GS9 of color A / B / C respectively ; : A31[6:0] / B31[6:0] / C31[6:0]: Gamma Setting for GS61 of color A / B / C respectively. A32[6:0] / B32[6:0] / C32[6:0]: Gamma Setting for GS63 of color A / B / C respectively. The Gamma Setting of GS2, GS4, GS6,…, GS58, GS60, GS62 are derived automatically by the driver based on this formula: GSn = (GSn-1 + GSn+1) / 2 , for n= 2,4,…,60,62 and division remainder is truncated. The gray scale is defined in incremental way, with reference to the length of previous table entry: Setting of GS1 must > 0 Setting of GS3 must > Setting of GS1 +1 Setting of GS5 must > Setting of GS3 +1 : Setting of GS63 must > Setting of GS61 +1											

BE h	GLUT (Gamma Look Up Table)

The following is an example of setting the GLUT:

1. Define the odd entry pulse widths that comply with the above conditions:

Gray Scale	Gamma Setting
GS1	3
GS3	7
GS5	23
:	:
GS59	108
GS61	115
GS63	127

2. Enter the Gamma Setting from GS1, GS3, GS5,…, GS59, GS61, GS63 one by one in sequence following the command BEh during the software initialization.

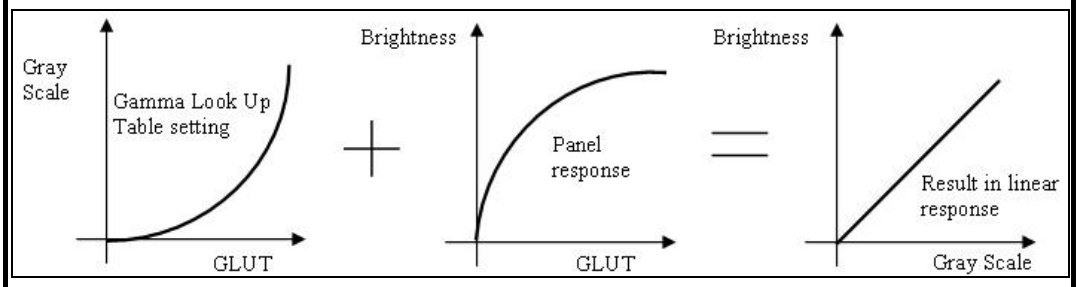
Then the driver automatically derives the Gamma setting of the even entry : GS2, GS4, …,GS60, GS62 with the previous mentioned formula:

Gray Scale	Formula	Gamma Setting
GS2	(GS1+GS3)/2=(3+7)/2=5	5
GS4	(GS3+GS5)/2=(7+23)/2=15	15
:	:	
GS60	(GS59+GS61)/2=(108+115)/2=111.5	111
GS62	(GS61+GS63)/2=(115+127)/2=121	121

Note
(1) Input 1d for Gamma Setting 1, 2d for Gamma setting 2, ... ,127d for Gamma Setting127

The setting of Gray Scale entry can perform Gamma correction on OLED panel display. Normally, it is desired that the brightness response of the panel is linearly proportional to the image data value in display data RAM. However, the OLED panel is somehow responded in non-linear way. Appropriate Gray Scale table setting like example below can compensate this effect.

Figure 9-12 : Example of Gamma correction by Gamma Look Up table setting



Default	Status	Default Value
	H/W Reset	Linear GLUT (B9h)

9.3.39 Set Display Offset (C8h)

C8 h	SETDO (Set Display Offset)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	0	0	C8
1st Parameter	1	1	↑	A7	A6	A5	A4	A3	A2	A1	A0	00..9F (1)

Description

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-159. For example, to move the COM16 towards the COM0 direction for 16 lines, A[7:0] should be given by 00010000. The figure below shows an example of this command. In there, "Row" means the graphic display data RAM row.

Figure 9-13 : Example of Set Display Start Line with no Remap (i.e. Command 36h bit A7=0b)

	a	b	c	Case
	160	96	96	MUX ratio (CAh)
	0	0	32	Display offset (C8h A[7:0])
COM0	Row0	Row0	Row32	
COM1	Row1	Row1	Row33	
COM2	Row2	Row2	Row34	
:	:	:	:	
COM61	Row61	Row61	Row93	
COM62	Row62	Row62	Row94	
COM63	Row63	Row63	Row95	
COM64	Row64	Row64	-	
COM65	Row65	Row65	-	
COM66	Row66	Row66	-	
:	:	:	:	
COM93	Row93	Row93	-	
COM94	Row94	Row94	-	
COM95	Row95	Row95	-	
COM96	Row96	-	-	
COM97	Row97	-	-	
COM98	Row98	-	-	
:	:	:	:	
COM124	Row124	-	-	
COM125	Row125	-	-	
COM126	Row126	-	-	
COM127	Row127	-	Row0	
COM128	Row128	-	Row1	
COM129	Row129	-	Row2	
:	:	:	:	
COM157	Row157	-	Row29	
COM158	Row158	-	Row30	
COM159	Row159	-	Row31	
Display example	 (a)	 (c)	 (d)	 (GDDARAM)

Restriction

Note

(1) A[7:0] + MUX ratio must be less than or equal to 160d. That means when MUX ratio is set to 160, this command is not recommend to use.

(2) MUX ratio can be set by command CAh,

Default

Status	Default Value
H/W Reset	A[7:0]=00h

9.3.40 Horizontal Scrolling (C9h)

C9 h	HORSCR (Horizontal Scrolling)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	0	1	C9
1st Parameter	1	1	↑	xx	A6	A5	A4	A3	A2	A1	A0	00..7F

Description

This command performs the horizontal scrolling through mapping one of the columns in the graphic display data RAM to SEG0.

A[6:0]	Number of column in horizontal scroll
00h	No horizontal scroll
01h	RAM column address 1 maps to SEG0
02h	RAM column address 2 maps to SEG0
03h	RAM column address 3 maps to SEG0
:	:
7Fh	Last RAM column address 7F maps to SEG0

The figure below shows examples of this command. In there, "Col" means the graphic display data RAM column.

A[6:0]	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	...	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127
0	Col 0	Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	...	Col 122	Col 123	Col 124	Col 125	Col 126	Col 127
2	Col 2	Col 3	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	...	Col 124	Col 125	Col 126	Col 127	Col 0	Col 1
4	Col 4	Col 5	Col 6	Col 7	Col 8	Col 9	Col 10	Col 11	...	Col 126	Col 127	Col 0	Col 1	Col 2	Col 3
127	Col 127	Col 0	Col 1	Col 2	Col 3	Col 4	Col 5	Col 6	...	Col 121	Col 122	Col 123	Col 124	Col 125	Col 126
125	Col 125	Col 126	Col 127	Col 0	Col 1	Col 2	Col 3	Col 4	...	Col 119	Col 120	Col 121	Col 122	Col 123	Col 124
123	Col 123	Col 124	Col 125	Col 126	Col 127	Col 0	Col 1	Col 2	...	Col 117	Col 118	Col 119	Col 120	Col 121	Col 122

The following code shows example of horizontal scrolling towards SEG0:

```
for n = 1 to 127
  Command    C9h        \\ Horizontal Scrolling command
  Data       n          \\ RAM column address n maps to SEG0
  Insert time interval between each scroll step
end
```

Default

Status	Default Value
H/W Reset	A[6:0]=00h

9.3.41 Set MUX ratio (CAh)

CA h	SETMUX (Set MUX ratio)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	0	0	1	0	1	0	CA
1st Parameter	1	1	↑	A7	A6	A5	A4	A3	A2	A1	A0	0F..9F
Description	Set MUX ratio to N+1 MUX N = A[7:0] from 15d to 159d (i.e.16MUX -160 MUX) A[7:0] from 00d to 14d are invalid entry											
Default												

Status	Default Value
H/W Reset	A[7:0]=9Fh (i.e. 160MUX)

9.3.42 Set Phase Length (CDh)

<table>
<tr><th>CD h</th><th colspan="12">PHLEN (Set Phase Length)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>CD</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>00..FF</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to set the OLED driving waveform length in phase 1 and phase 2.
The A[3:0] defines the Phase 1 period of 5~31 DCLK clocks as follow:
<table><tr><td>A[3:0]</td><td>Phase 1 period</td></tr><tr><td>0000</td><td>invalid</td></tr><tr><td>0001</td><td>invalid</td></tr><tr><td>0010</td><td>5 DCLKs</td></tr><tr><td>0011</td><td>7 DCLKs</td></tr><tr><td>0100</td><td>9 DCLKs [reset]</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111</td><td>31 DCLKs</td></tr></table>
The A[7:4] defines the Phase 2 period of 3~15 DCLK clocks as follow:
<table><tr><td>A[7:4]</td><td>Phase 2 period</td></tr><tr><td>0000</td><td>invalid</td></tr><tr><td>0001</td><td>invalid</td></tr><tr><td>0010</td><td>invalid</td></tr><tr><td>0011</td><td>3 DCLKs</td></tr><tr><td>0100</td><td>4 DCLKs</td></tr><tr><td>:</td><td>:</td></tr><tr><td>0111</td><td>7 DCLKs[reset]</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111</td><td>15 DCLKs</td></tr></table>
Refer to section 8.7 for details of phase 1 & phase 2.</td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>H/W Reset</td><td>A[3:0]=4h, A[7:4]=7h</td></tr></table></td></tr>
</table>

9.3.43 Set Second Precharge Period (CEh)

<table>
<tr><th>CE h</th><th colspan="11">SECPLEN (Set Second Precharge Period)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>CE</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command sets the second precharge period as follow:

<table><tr><td>A[3:0]</td><td>second Precharge Period</td></tr><tr><td>0000</td><td>0 DCLK</td></tr><tr><td>0001</td><td>1 DCLK</td></tr><tr><td>0010</td><td>2 DCLKs</td></tr><tr><td>:</td><td>:</td></tr><tr><td>0111</td><td>7 DCLKs [reset]</td></tr><tr><td>:</td><td>:</td></tr><tr><td>1111</td><td>15 DCLKs</td></tr></table>
Refer to section 8.7 for details of second precharge.</td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>H/W Reset</td><td>A[3:0]=0111</td></tr></table></td></tr>
</table>

9.3.44 Set Second Precharge speed (CFh)

<table>
<tr><th>CF h</th><th colspan="11">SSPS (Set Second Precharge speed)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td><td>CF</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>0</td><td>A1</td><td>A0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">Set Second Precharge speed

A[1:0]= 00b, Second Pre-charge speed =slowest
A[1:0]= 01b, Second Pre-charge speed =slow
A[1:0]= 10b, Second Pre-charge speed =normal [reset]
A[1:0]= 11b, Second Pre-charge speed =Fast

Refer to section 8.7 for details of second precharge.</td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><td>Status</td><td>Default Value</td></tr><tr><td>H/W Reset</td><td>A[1:0]= 10b</td></tr></table></td></tr>
</table>

9.3.45 Set Display Clock Divider / Oscillator Frequency (D2h)

<table>
<tr><th>D2 h</th><th colspan="11">SDCOSCF (Set Display Clock Divider / Oscillator Frequency)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>D2</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">A[3:0] Display Clock (DCLK) Divider

<table><tr><th>A[3:0]</th><th>Divider</th></tr><tr><td>0000</td><td>divide by 1</td></tr><tr><td>0001</td><td>divide by 2</td></tr><tr><td>0010</td><td>divide by 4</td></tr><tr><td>0011</td><td>divide by 8</td></tr><tr><td>0100</td><td>divide by 16</td></tr><tr><td>0101</td><td>divide by 32</td></tr><tr><td>0110</td><td>divide by 64</td></tr><tr><td>0111</td><td>divide by 128</td></tr><tr><td>1000</td><td>divide by 256</td></tr><tr><td>1001</td><td>divide by 512</td></tr><tr><td>1010</td><td>divide by 1024</td></tr><tr><td>>=1011</td><td>invalid</td></tr></table>
DCLK is generated from CLK divided by Divider

A[7:4] F_{OSC} frequency
F_{OSC} stands for frequency value of the internal oscillator
Frequency increases as setting value increases

Refer to section 8.5 for details.</td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>H/W Reset</td><td>A[7:4] =1100b, A[3:0]=0000b</td></tr></table></td></tr>
</table>

9.3.46 Set V_{COMH} (D3h)

<table>
<tr><th>D3 h</th><th colspan="11">SETVCOMH (Set V_{COMH})</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>D3</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A2</td><td>A1</td><td>A0</td><td>00..07</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to set the V_{COMH} as followed:

<table>
<tr><td>A[2:0]</td><td>V_{COMH}</td></tr>
<tr><td>000</td><td>0.72*V_{CC}</td></tr>
<tr><td>001</td><td>0.74*V_{CC}</td></tr>
<tr><td>010</td><td>0.76*V_{CC}</td></tr>
<tr><td>011</td><td>0.78*V_{CC}</td></tr>
<tr><td>100</td><td>0.80*V_{CC} [reset]</td></tr>
<tr><td>101</td><td>0.82*V_{CC}</td></tr>
<tr><td>110</td><td>0.84*V_{CC}</td></tr>
<tr><td>111</td><td>0.86*V_{CC}</td></tr>
</table></td></tr>
<tr><td>Default</td><td colspan="12">
<table>
<tr><td>Status</td><td>Default Value</td></tr>
<tr><td>H/W Reset</td><td>A[2:0]=100b</td></tr>
</table></td></tr>
</table>

9.3.47 GPIO (D7h)

<table>
<tr><th>D7 h</th><th colspan="12">GPIO (General Purpose IO)</th></tr>
<tr><td></td><td>D/C#</td><td>RD#</td><td>WR#</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>0</td><td>1</td><td>↑</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>D7</td></tr>
<tr><td>1st Parameter</td><td>1</td><td>1</td><td>↑</td><td>xx</td><td>xx</td><td>xx</td><td>xx</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>xx</td></tr>
<tr><td>Description</td><td colspan="12">This command is used to enable or disable the GPIO0 pin and GPIO1 pin.

For GPIO0 pin:
<table><tr><th>D[1:0]</th><th>Description</th></tr><tr><td>00</td><td>GPIO0 pin high impedance (HiZ). Input disabled (always read as low) [reset]</td></tr><tr><td>01</td><td>GPIO0 pin HiZ, Input enabled</td></tr><tr><td>10</td><td>GPIO0 pin output LOW</td></tr><tr><td>11</td><td>GPIO0 pin output HIGH</td></tr></table>
For GPIO1 pin:
<table><tr><th>D[3:2]</th><th>Description</th></tr><tr><td>00</td><td>GPIO1 pin high impedance (HiZ). Input disabled (always read as low) [reset]</td></tr><tr><td>01</td><td>GPIO1 pin HiZ, Input enabled</td></tr><tr><td>10</td><td>GPIO1 pin output LOW</td></tr><tr><td>11</td><td>GPIO1 pin output HIGH</td></tr></table>
Note
(1) Input disabled means floating input is allowed.</td></tr>
<tr><td>Default</td><td colspan="12"><table><tr><th>Status</th><th>Default Value</th></tr><tr><td>H/W Reset</td><td>D[3:2]=00, D[1:0]= 00</td></tr></table></td></tr>
</table>

9.3.48 Command Lock (FDh)

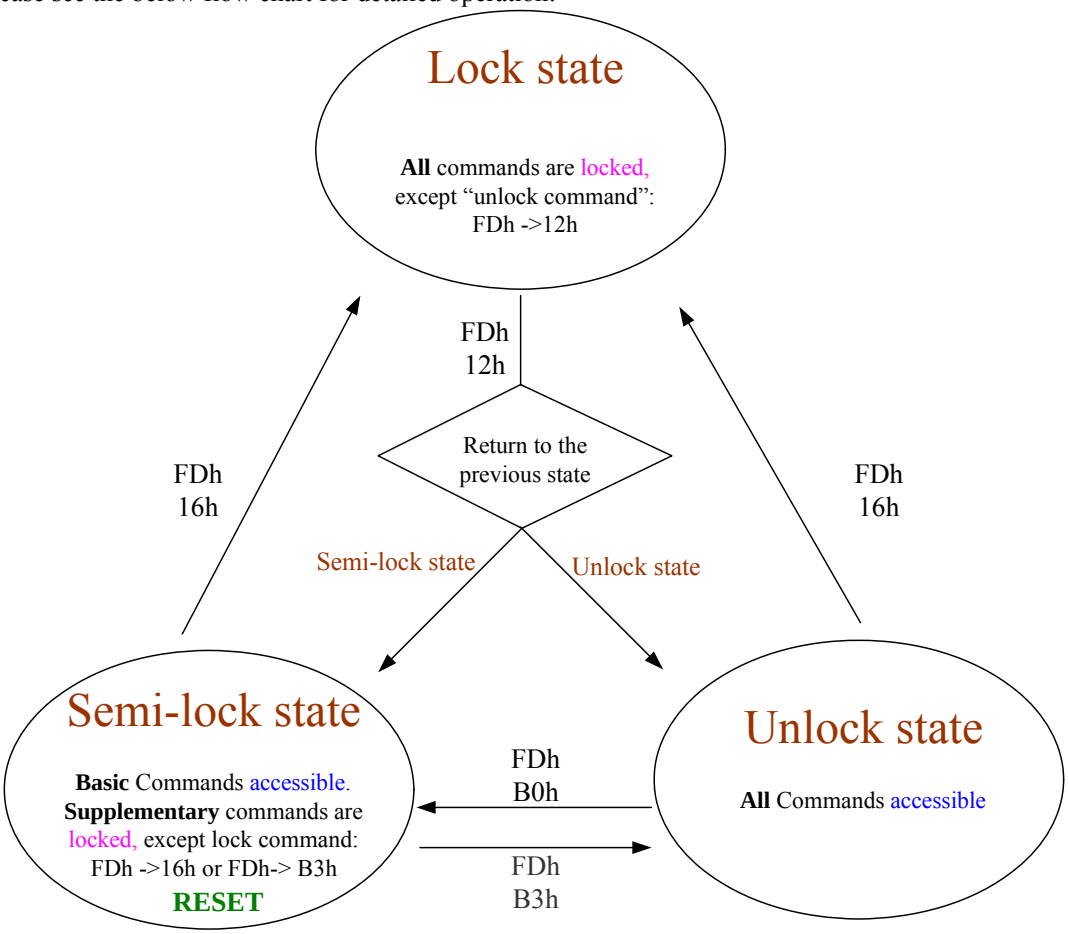
FD h	CMDLCK (Command Lock)											
	D/C#	RD#	WR#	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	0	1	↑	1	1	1	1	1	1	0	1	FD
Parameter	1	1	↑	A7	A6	A5	A4	A3	A2	A1	A0	xx

Description

This command is design to prevent change of command set value. This helps to prevent accidental/unintentional access to change important or factory configuration during normal operation. Level of command lock can be to lock only basic commands (00h to 52h, DAh), and also lock supplementary commands (usually for factory setting) (B1h to D7h, FDh). Please refer to section 9.1 and 9.2 for the list of basic commands and supplementary commands.

A[7:0]	Description
12h	Unlock basic commands. Basic command can be accessed.
16h	Lock all commands. All commands can not be accessed, except command: FDh ->12h can be used to unlock basic command.
B0h	Lock all supplementary command. In this state, for supplementary command access, only FDh ->16hcommand can be sent.
B3h	Unlock supplementary commands. All supplementary commands can be accessed.
other values	Invalid

Please see the below flow chart for detailed operation:



Default

Status	Default Value
H/W Reset	Semi-lock state

10 MAXIMUM RATINGS

Table 10-1 : Maximum Ratings

(Voltage Reference to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to 2.75	V
V_{CC}		-0.5 to 22.0	V
V_{DDIO}		-0.5 to V_{CI}	V
V_{CI}		-0.3 to 4.0	V
V_{SEG}	SEG output voltage	0 to V_{CC}	V
V_{COM}	COM output voltage	0 to 0.9*V_{CC}	V
V_{in}	Input voltage	Vss-0.3 to V_{DDIO}+0.3	V
T_A	Operating Temperature	-40 to +85	ºC
T_{stg}	Storage Temperature Range	-65 to +150	ºC

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

Conditions (Unless otherwise specified)

Voltage referenced to V_{SS}, V_{DDIO} = 2.8V, V_{DD} = 2.4V ~ 2.6V, V_{CI} = 2.8V, T_A = 25°C

Table 11-1 : DC Characteristics

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
V_{CC}	Operating Voltage	-		10	-	21	V
V_{DD}	Logic Supply Voltage	-		2.4	-	2.6	V
V_{CI}	Low voltage power supply	-		2.4	-	3.5	V
V_{DDIO}	Power Supply for I/O pins	-		1.6	-	V_{CI}	V
V_{OH}	High Logic Output Level	Iout =100uA		0.9*V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low Logic Output Level	Iout =100uA		0	-	0.1*V_{DDIO}	V
V_{IH}	High Logic Input Level	-		0.8*V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low Logic Input Level	-		0	-	0.2*V_{DDIO}	V
I_{SLP_VDD}	V_{DD} Sleep mode Current	V_{CI} = V_{DDIO} =2.8V, V_{CC} =16V V_{DD}(external) = 2.5V, Display OFF, No panel attached		-	-	10	uA
I_{SLP_VDDIO}	V_{DDIO} Sleep mode Current	V_{CI} = V_{DDIO} =2.8V, V_{CC} =16V Display OFF, No panel attached	External V_{DD} = 2.5V	-	-	10	uA
			Internal V_{DD}	-	-	10	uA
I_{SLP_VCC}	V_{CC} Sleep mode Current	V_{CI} = V_{DDIO} =2.8V, V_{CC} =16V Display OFF, No panel attached	External V_{DD} = 2.5V	-	-	10	uA
			Internal V_{DD}	-	-	10	uA
I_{SLP_VCI}	V_{CI} Sleep mode Current	V_{CI} = V_{DDIO} =2.8V, V_{CC} =16V Display OFF, No panel attached	External V_{DD} = 2.5V	-	-	10	uA
			Enable Internal V_{DD} during Sleep mode	-	-	70	uA
			Disable Internal V_{DD} during Sleep mode	-	-	10	uA
I_{DD}	V_{DD} Supply Current	V_{CI} = V_{DDIO} =2.8V, V_{CC} = 16V, External V_{DD} = 2.5V, Display ON, No panel attached, contrast = FF		-	650	720	uA
I_{DDIO}	V_{DDIO} Supply Current	V_{CI} = V_{DDIO} =, 2.8V, V_{CC} = 16, Display ON, No panel attached, contrast = FF	External V_{DD} = 2.5V	-	0.5	10	uA
			Internal V_{DD}	-	0.5	10	uA
I_{CI}	V_{CI} Supply Current	V_{CI} = V_{DDIO} =, 2.8V, V_{CC} = 16, Display ON, No panel attached, contrast = FF	External V_{DD} = 2.5V	-	-15	-9	uA
			Internal V_{DD}	-	670	750	uA
I_{CC}	V_{CC} Supply Current	V_{CI} = V_{DDIO} =, 2.8V, V_{CC} = 16, Display ON, No panel attached, contrast = FF	External V_{DD} = 2.5V	-	1.65	1.9	mA
			Internal V_{DD}	-	1.65	1.9	mA
I_{SEG}	Segment Output Current Setting V_{CC} = 21 I_{REF} = 13.5uA	Contrast = FFh , GS63 = Setting 127		-	230	250	uA
		Contrast = 7Fh, GS63 = Setting 127		-	120	-	uA
		Contrast = 3Fh, GS31 = Setting 63		-	62	-	uA
Dev	Segment (SA, SB, SC) output current uniformity (contrast = FF)	Dev = (I_{Sn} – I_{MID})/I_{MID} I_{MID} = (I_{MAX} + I_{MIN})/2 I_{Sn} = Segment n current . e.g. For n=A, then I_{Sn} = I_{SA} = SA current	n = A	-3	-	3	%
			n = B	-3	-	3	
			n = C	-3	-	3	
Adj. Dev	Adjacent pin output current uniformity (contrast = FF)	Adj Dev = (I_{Sn}[m]-I_{Sn}[m+1]) / (I_{Sn} [m]+ I_{Sn} [m+1]) e.g. For n=A, m=3, then I_{Sn}[m]= I_{SA}[3] = SA[3] current	n = A	-2	-	2	%
			n = B	-2	-	2	
			n = C	-2	-	2	
I_{REF}	Segment output reference current	-		11.0	13.5	14.0	uA

12 AC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}
V_{DD} = 2.4V to 2.6V
V_{DDIO} = 2.8V
V_{CI} = 2.8V
T_A = 25°C

Table 12-1 : AC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
F_{OSC} (1)	Oscillation Frequency of Display Timing Generator	V_{CI} = 2.8V	1.28	1.43	1.6	MHz
F_{FRM}	Frame Frequency for 160 MUX Mode	128x160 Graphic Display Mode, Display ON, Internal Oscillator Enabled	-	F_{OSC} * 1/(D*K*160) (2)	-	Hz
t_{RES}	Reset low pulse width (RES#)	-	2000	-	-	ns

Note

(1) F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command D2h A[7:4] is in default value.

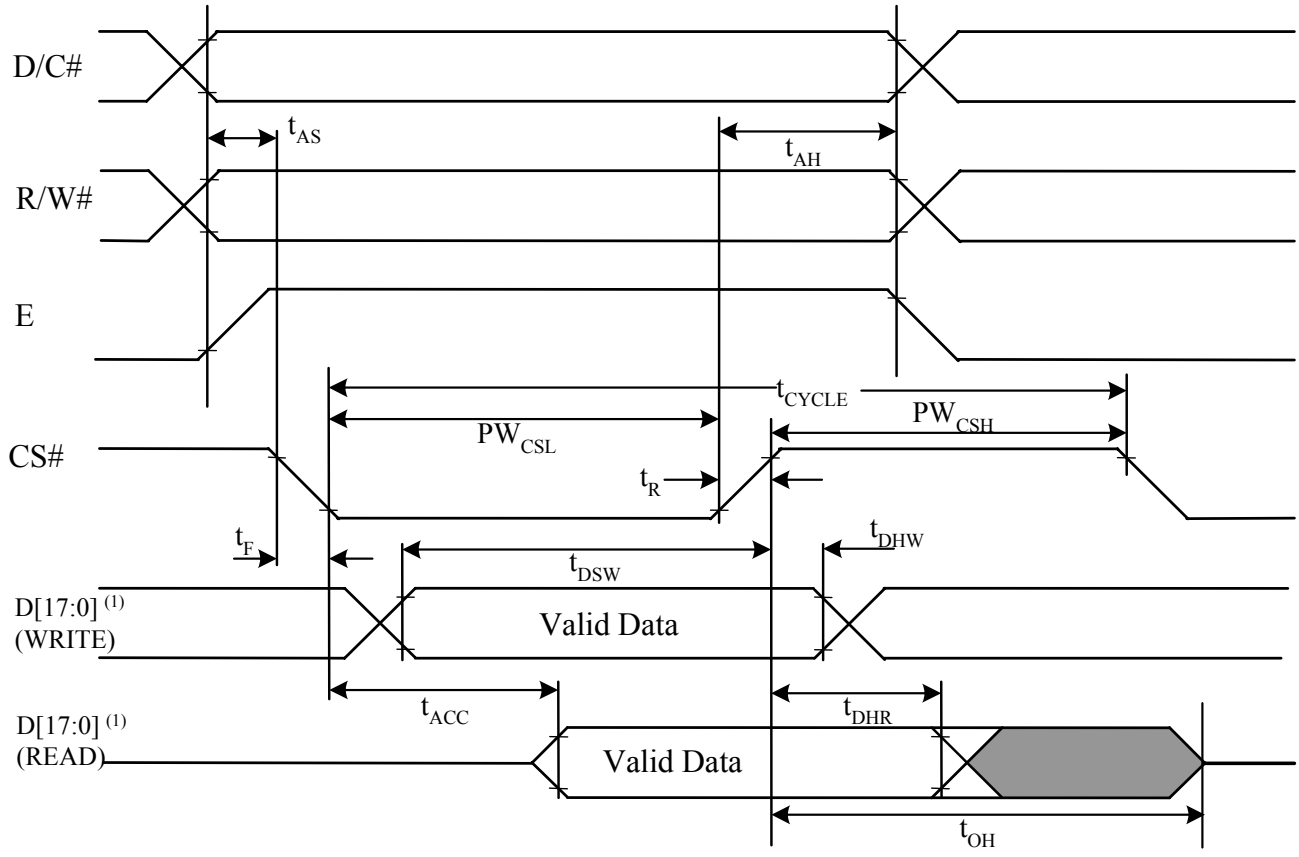
(2) D: divide ratio set by command D2h A[3:0]
K: Phase 1 period +Phase 2 period + 75

Table 12-2 : 6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 12-1 : 6800-series MCU parallel interface characteristics



Note

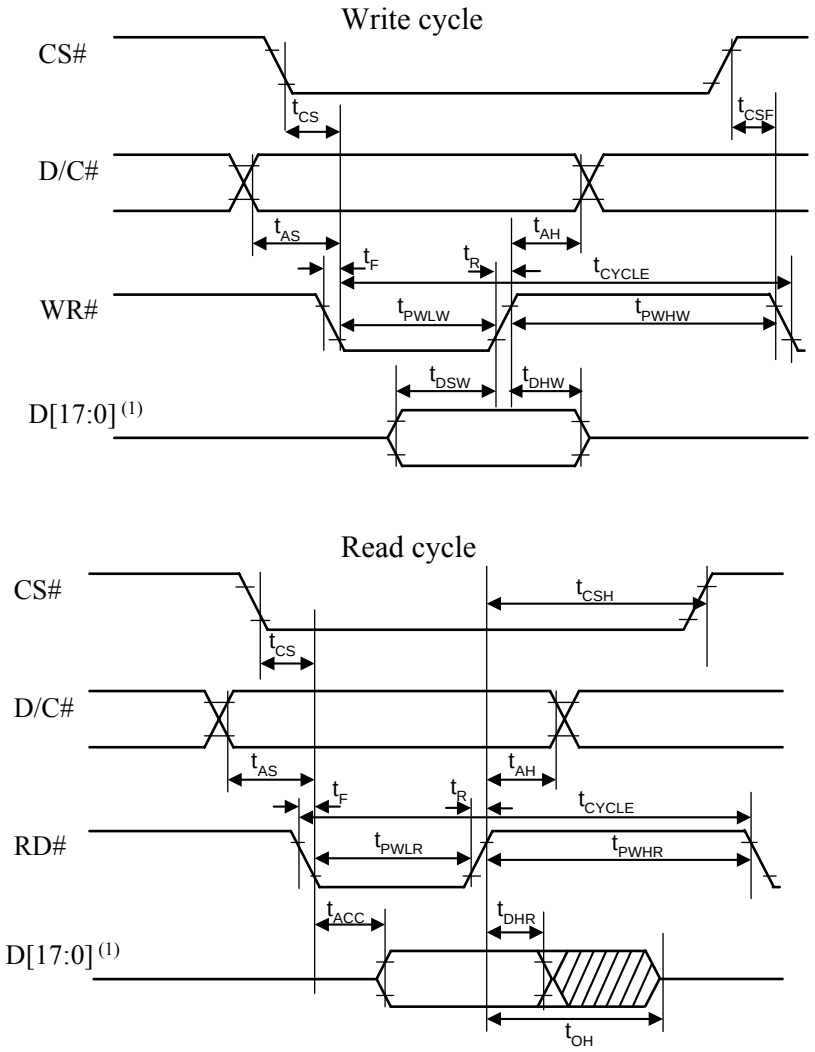
(1) when 8 bit used: D[7:0] instead; when 16 bit used: D[15:0] instead; when 18 bit used: D[17:0] instead.

Table 12-3 : 8080-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{CYCLE}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	150	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

Figure 12-2 : 8080-series MCU parallel interface characteristics



Note

(1) when 8 bit used: D[7:0] instead; when 16 bit used: [15:0] instead; when 18 bit used: D[17:0] instead.

Table 12-4 : Serial Interface Timing Characteristics (4-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

Figure 12-3 : Serial interface characteristics (4-wire SPI)

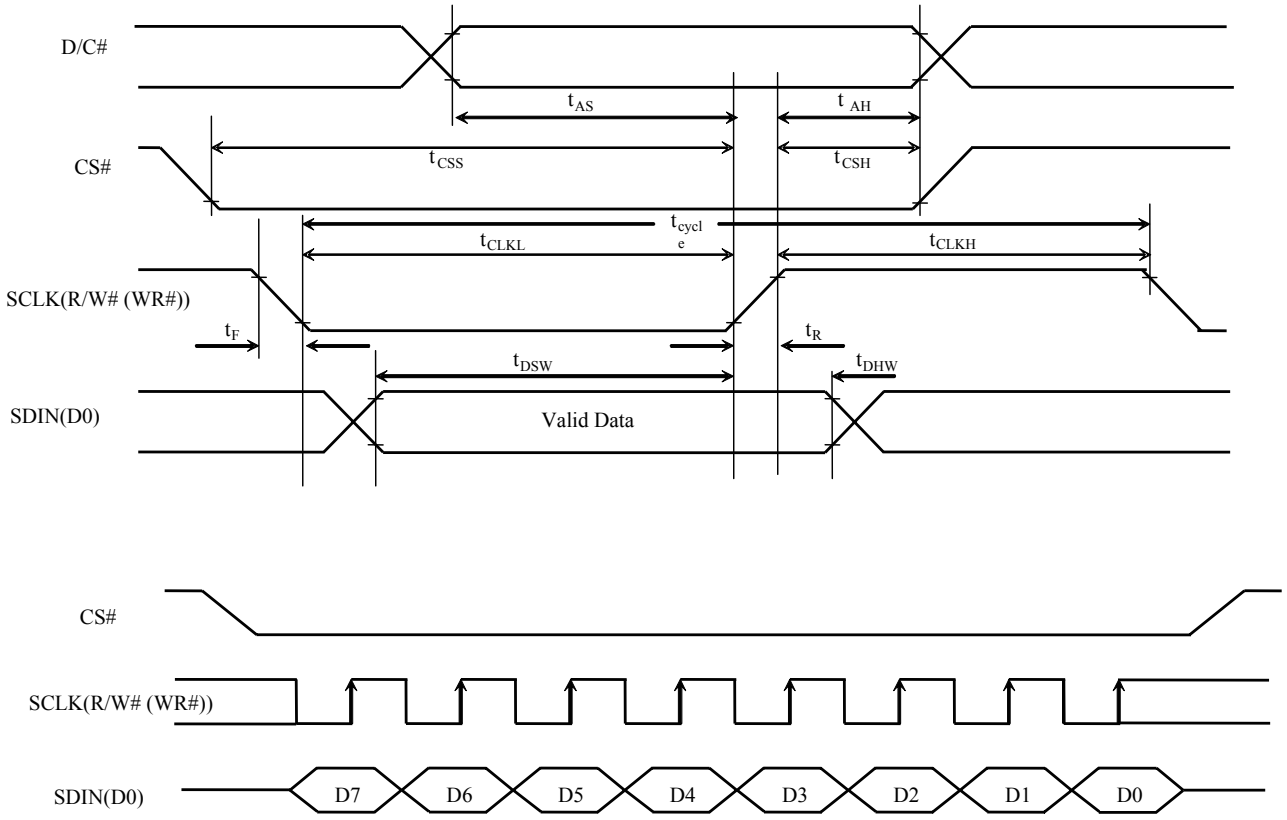
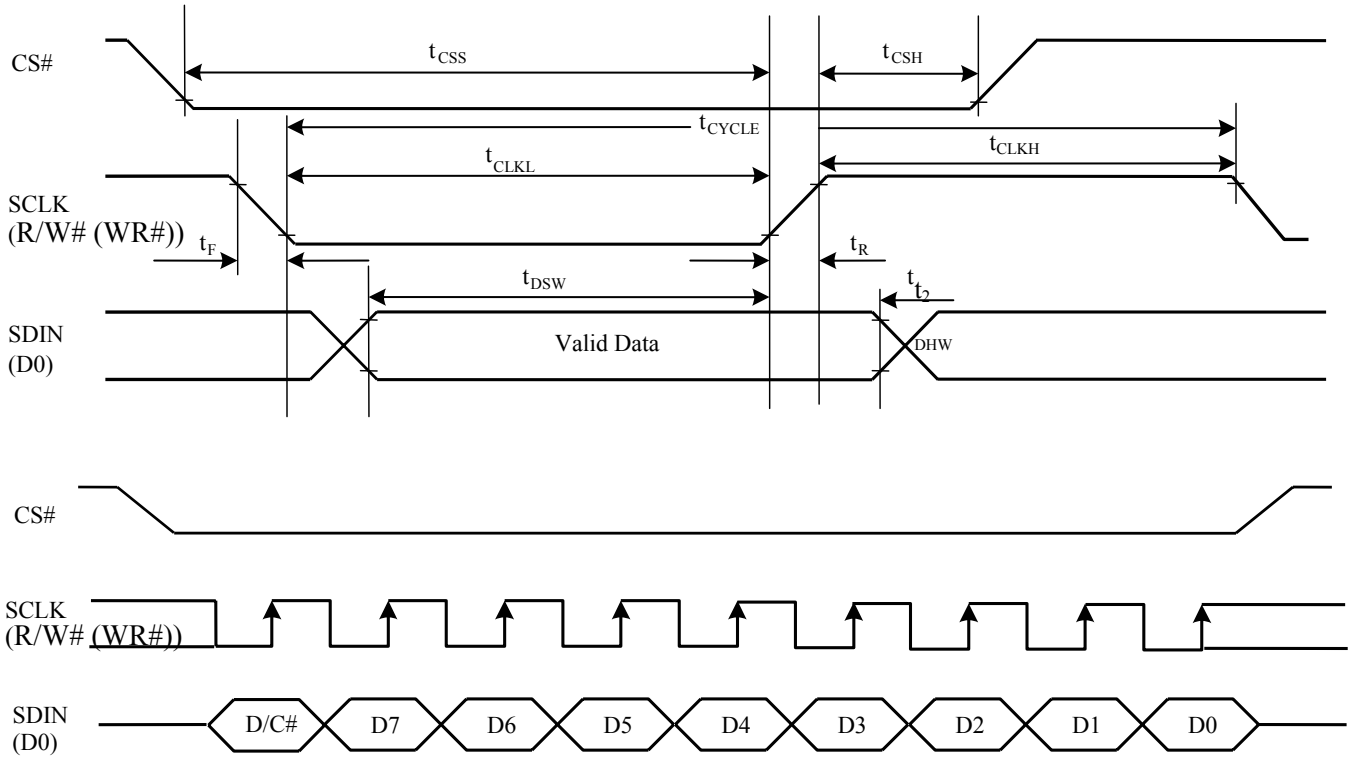


Table 12-5 : Serial Interface Timing Characteristics (3-wire SPI)

(V_{DD} - V_{SS} = 2.4 to 2.6V, V_{DDIO}=1.6V, V_{CI} = 2.8V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	50	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

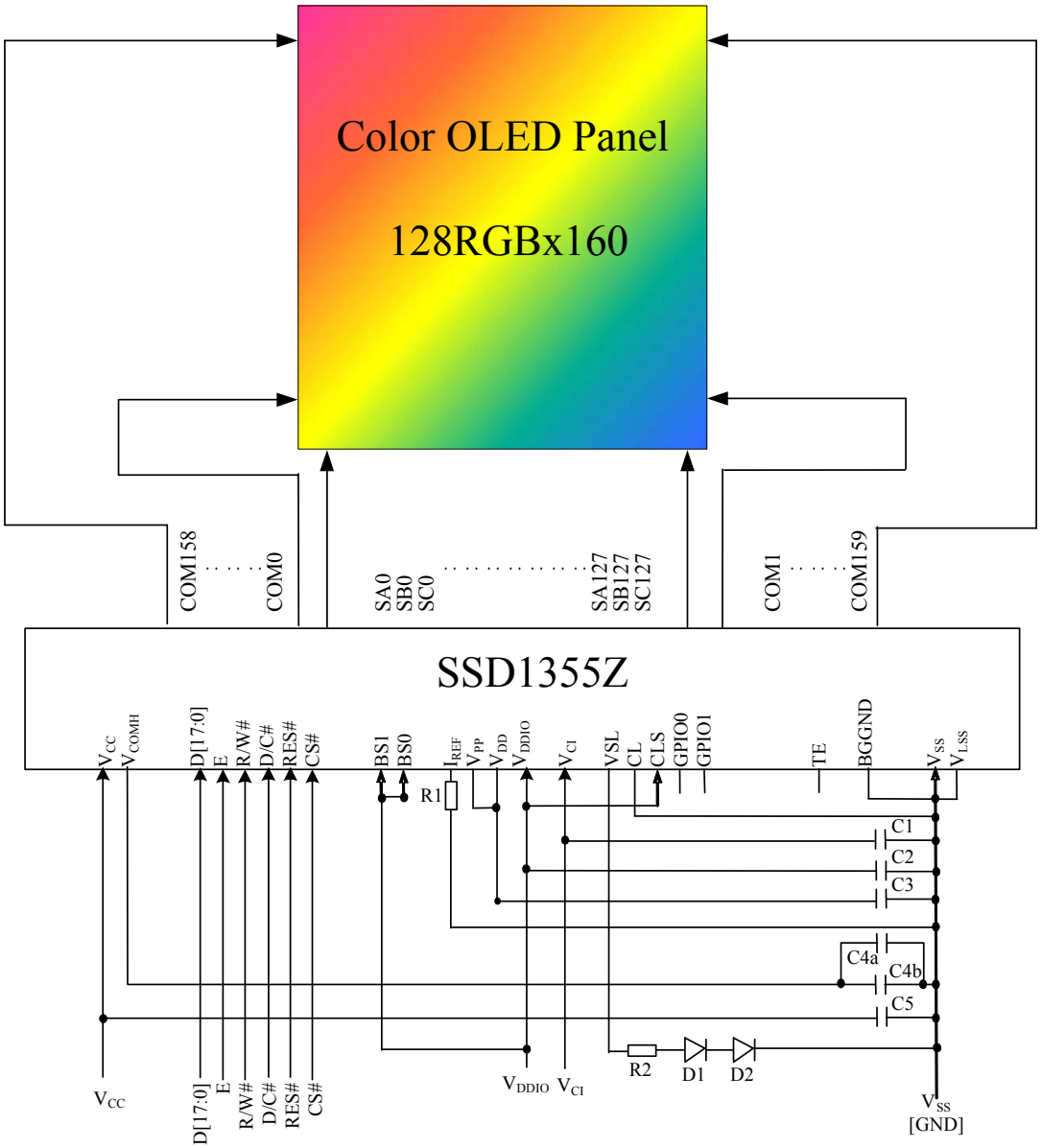
Figure 12-4 : Serial interface characteristics (3-wire SPI)



13 APPLICATION EXAMPLE

Figure 13-1 : SSD1355 application example for 18-bit 6800-parallel interface mode (Internal regulated V_{DD})

The configuration for 18-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram: (V_{CI} = 3.3V (V_{CI} must be > 2.6V), Internal regulated V_{DD} = 2.5V, V_{DDIO} = 1.8V, external V_{CC} = 18V, I_{REF} = 13.5uA, BS[3:2] are set to 11b through command 36h)



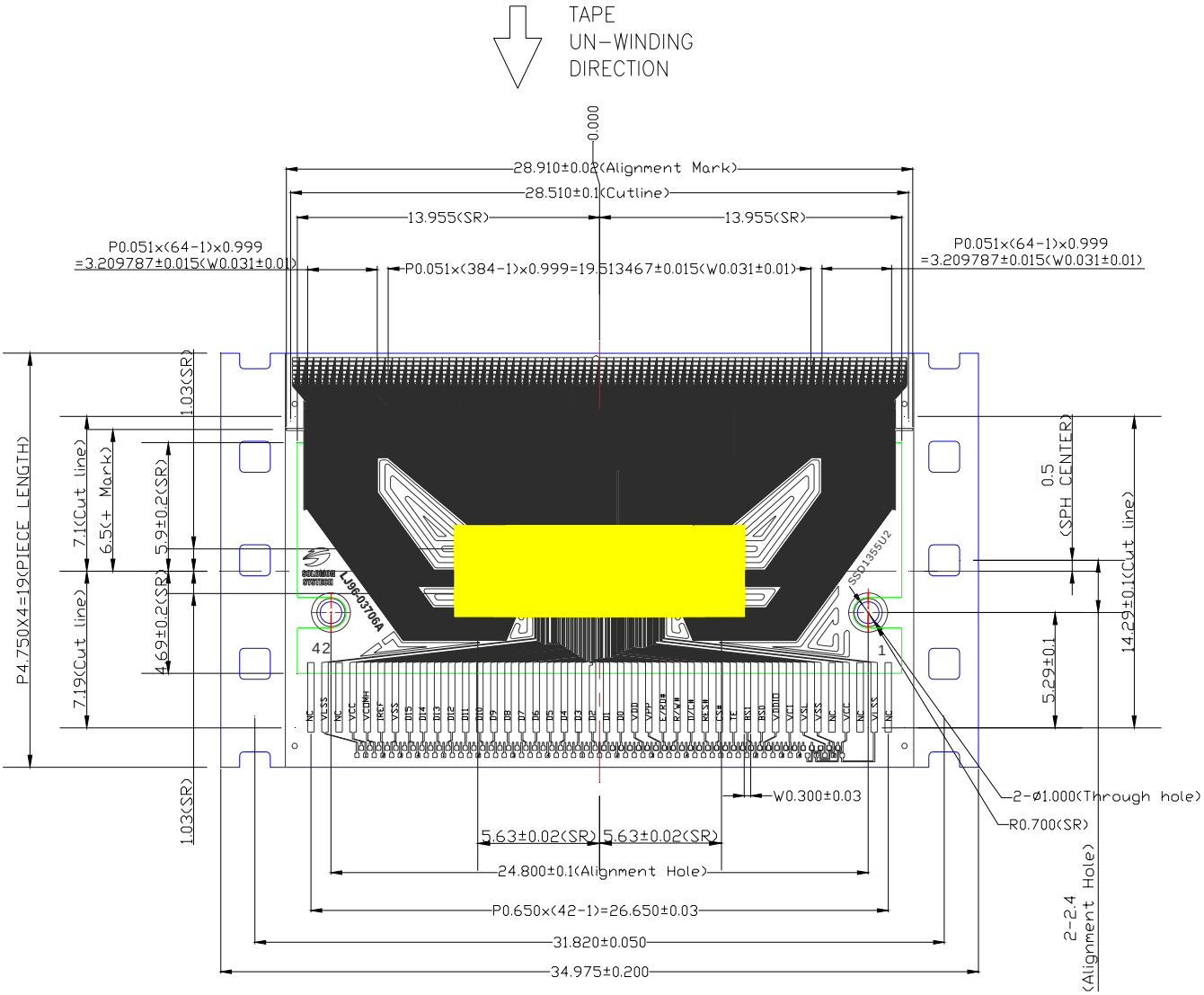
Voltage at I_{REF} = V_{CC} – 6V. For V_{CC} = 18V, I_{REF} = 13.5uA:
R1 = (Voltage at I_{REF} - V_{SS}) / I_{REF}
= (18-6) / 13.5u
= 880KΩ
R2 = 50Ω, 1/8W (1)
D1 ~ D2: V_{th}=0.7V, 1N4148 (1)
C1 ~ C3: 1uF, C4a, C5: 4.7uF, C4b: 0.1uF (1)

Note
(1) The values are recommended value. Select appropriate value against module application.

14 PACKAGE INFORMATION

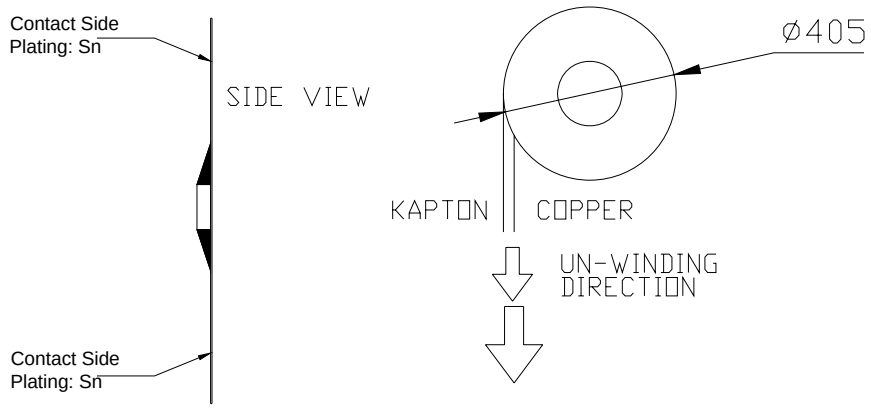
14.1 SSD1355U2R1 Detail Dimension

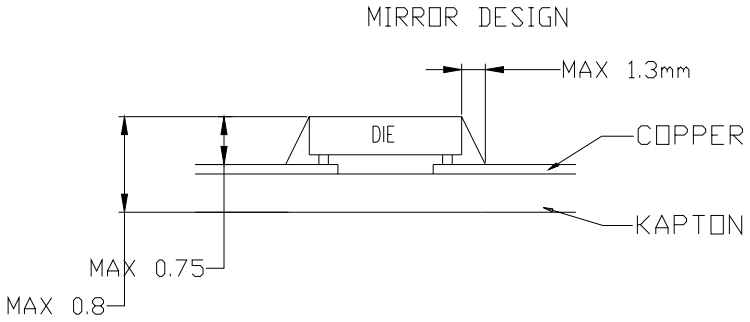
Figure 14-1 : SSD1355U2R1 Detail Dimension

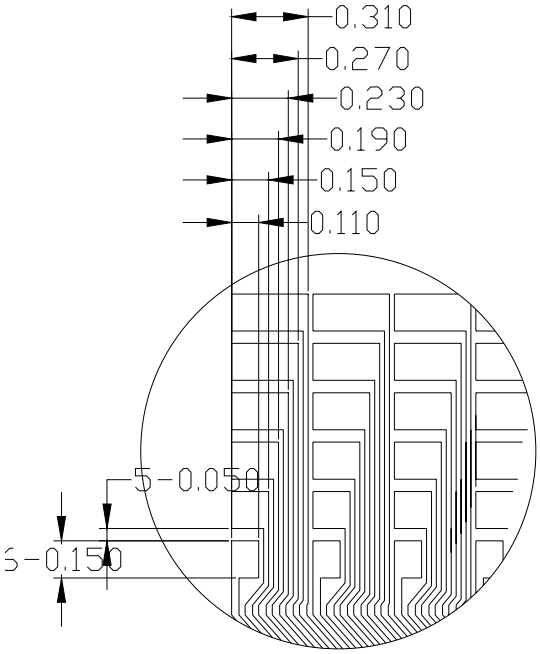


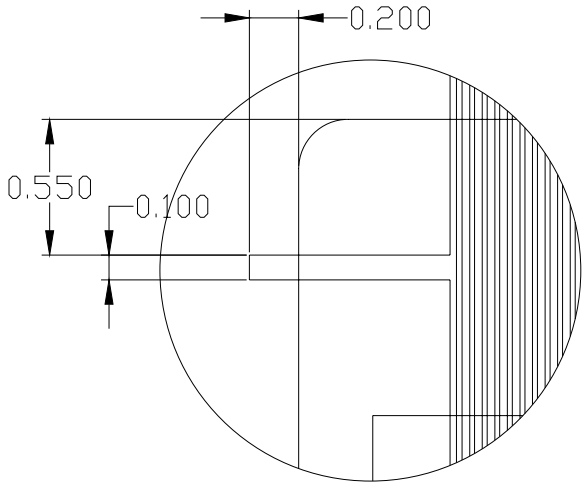
NOTE:

1. GENERAL TOLERANCE: ±0.050mm
2. MATERIAL
   PI: 38±4um
   CU: 8±2um
   SR: 10±5um
   (OTHER TOLERANCE: 0.200mm)
3. SN PLATING: 0.200±0.050um
4. TAPESIZE: 4 SPH, 19.00mm


Contact Side
Plating: Sn
SIDE VIEW
Contact Side
Plating: Sn
ø405
KAPTON
COPPER
UN-WINDING
DIRECTION

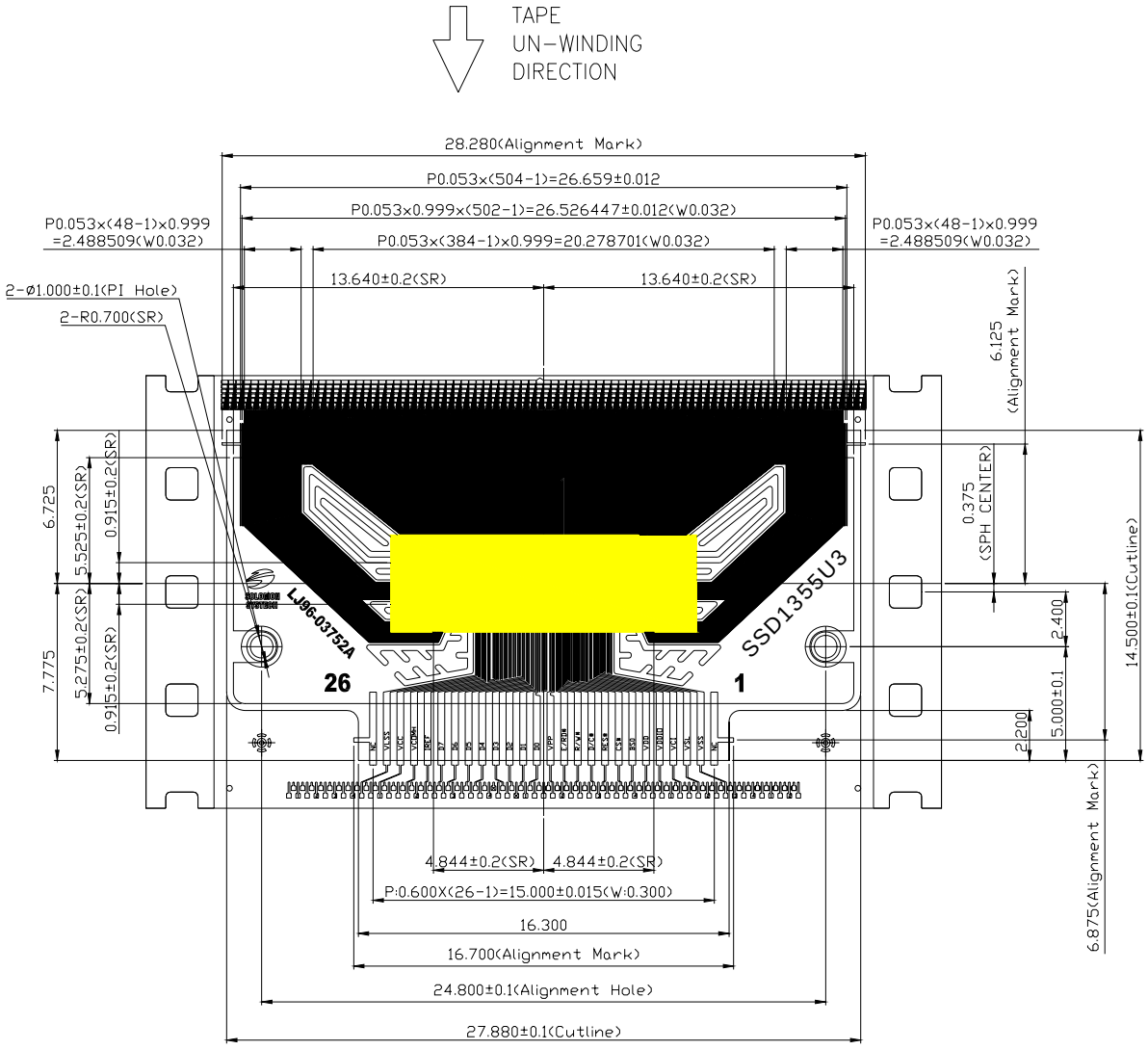

MIRROR DESIGN
MAX 1.3mm
DIE
COPPER
KAPTON
MAX 0.75
MAX 0.8


0.310
0.270
0.230
0.190
0.150
0.110
5-0.050
6-0.150

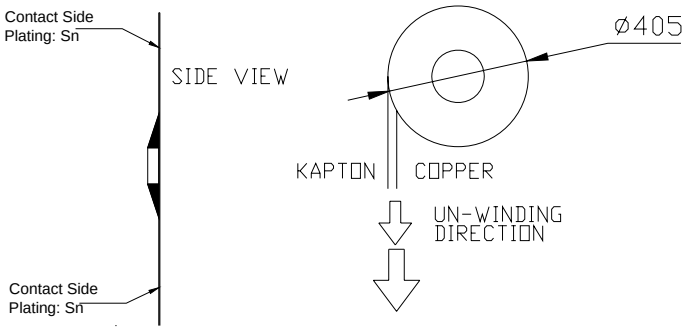

0.200
0.550
0.100

14.2 SSD1355U3R1 Detail Dimension

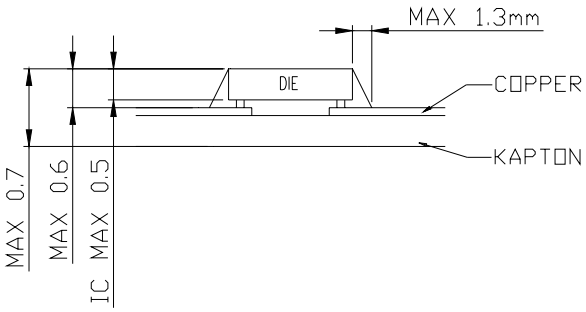
Figure 14-2 : SSD1355U3R1 Detail Dimension

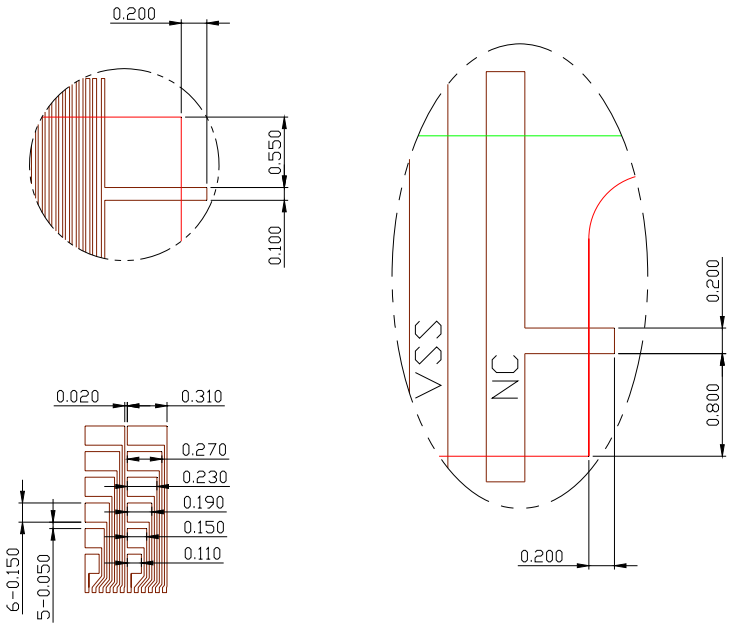


NOTE:
1. GENERAL TOLERANCE: ±0.050mm
2. MATERIAL
   PI: 38±4um
   CU: 8±2um
   SR: 10±5um
   (OTHER TOLERANCE: 0.200mm)
3. SN PLATING: 0.200±0.050um
4. TAPESIZE: 4 SPH, 19.00mm



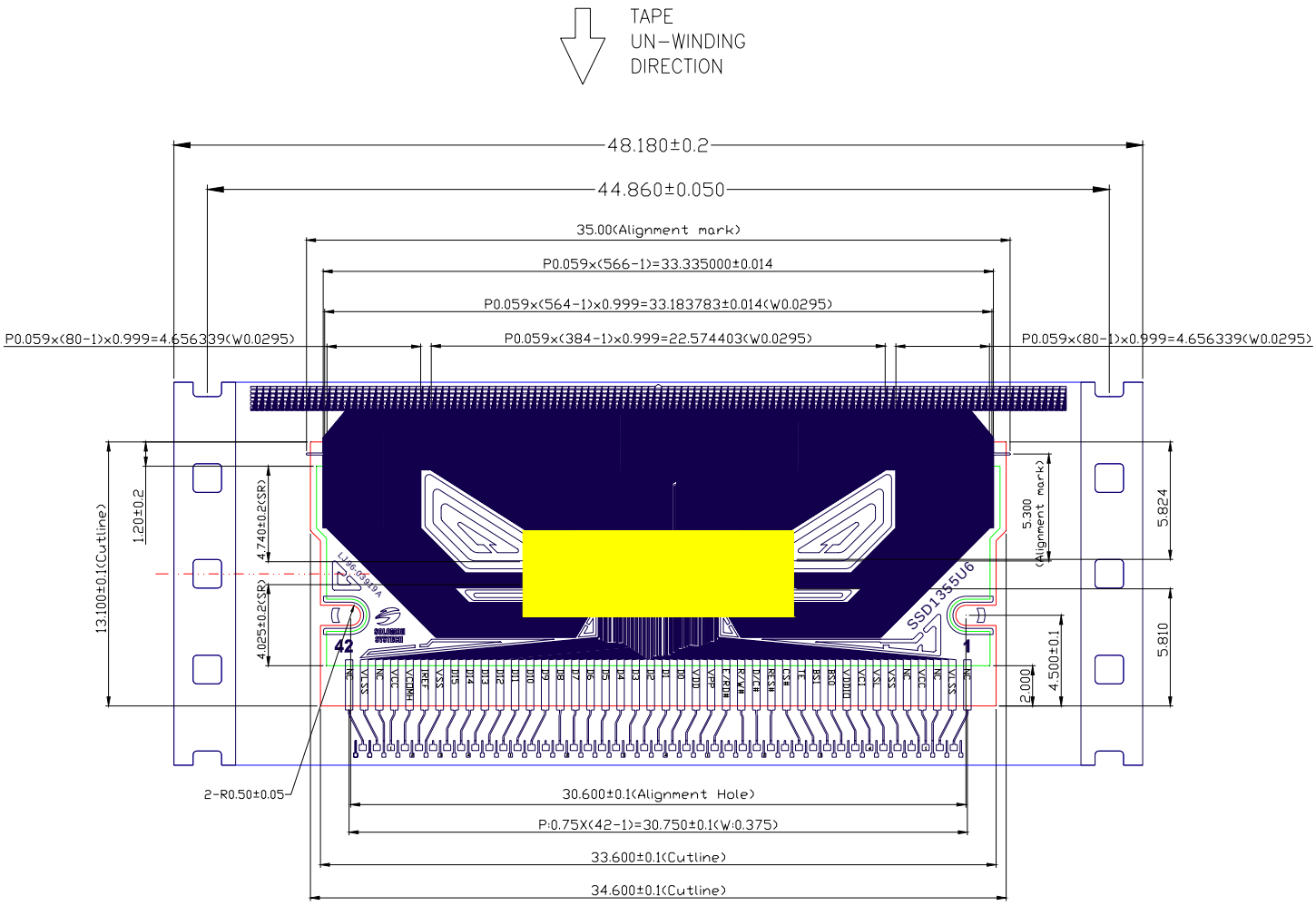
MIRROR DESIGN





14.3 SSD1355U6R1 Detail Dimension

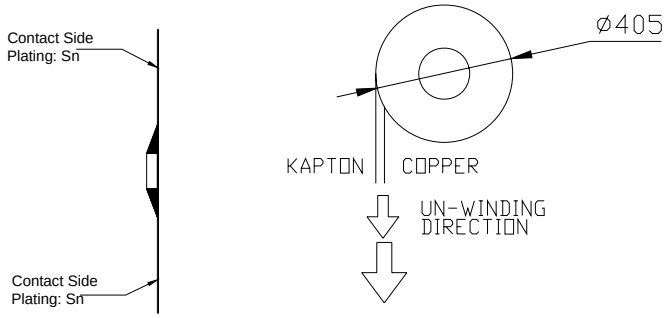
Figure 14-3 : SSD1355U6R1 Detail Dimension



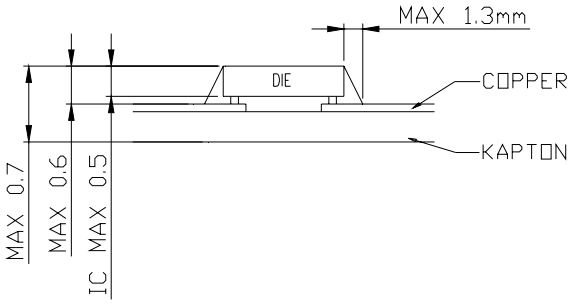
NOTE:

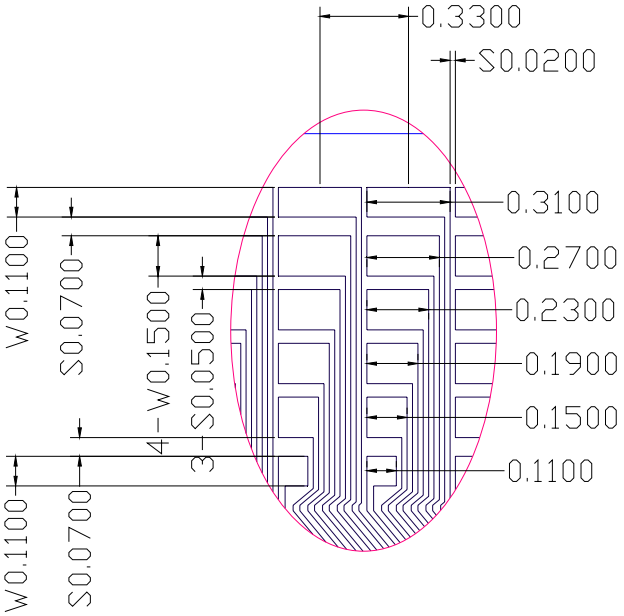
1. GENERAL TOLERANCE: ±0.050mm
2. MATERIAL
   PI: 38±4um
   CU: 8±2um
   SR: 10±5um
   (OTHER TOLERANCE: 0.200mm)
3. SN PLATING: 0.200±0.050um
4. TAPESIZE: 4 SPH, 19.00mm

SIDE VIEW



MIRROR DESIGN





All Solomon Systech Products complied with six (6) hazardous substances limitation requirement per European Union (EU) “Restriction of Hazardous Substance (RoHS) Directive (2002/95/EC)” and China standard “电子信息产品污染控制标识要求 (SJ/T11364-2006)” with control Marking Symbol . Hazardous Substances test report is available upon requested.

*http://www.solomon-systech.com*w